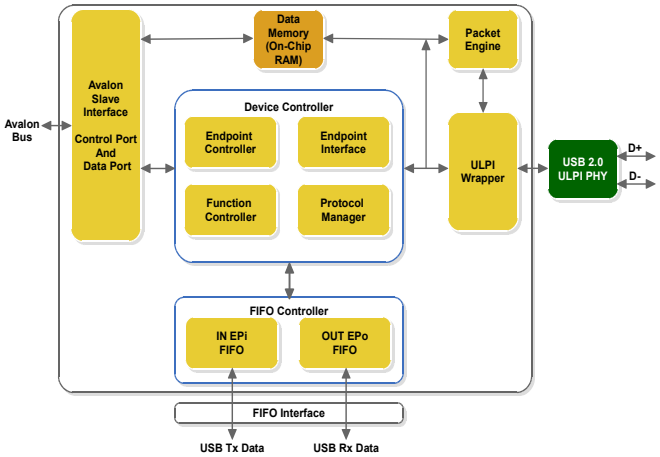
IP Core

USB 2.0 Device - Software Enumeration FIFO Interface (USB20SF)

The USB 2.0 Device, Software Enumeration FIFO interface (USB20SF) IP Core is a FIFO based USB 2.0 device core with 32-bit Avalon interface and ULPI interface support. The core supports both High Speed(480 Mbps) and Full Speed(12 Mbps) functionality. The core supports three preconfigured endpoints Control, IN, and OUT. It can be configured for up to 15 IN as well as OUT endpoints on customer's request at additional cost.

IP core has been implemented in Verilog HDL and its functionality has been verified using different test cases in simulation environment as well as on hardware. It is provided as Altera Qsys Ready component and hence can be easily integrated in Qsys system.

Architecture



Features

- Supports both Full Speed (12 Mbps) and High Speed (480 Mbps) modes
- Supports Control, Bulk, Interrupt and Isochronous transfers
- Capable to support up to 31 endpoints
  (1 default control endpoint + 15 IN/OUT endpoints)
- Supports software configurable endpoints
- Supports Suspend, Resume and Remote Wakeup features
- Supports UTMI + Low Pin interface (ULPI) interface
- Supports Asynchronous Avalon clock interface
- Preconfigured for 3 endpoints
  - CONTROL
  - IN
  - OUT
- Software controlled CONTROL endpoint
- Supports Asynchronous FIFO Interface for non CONTROL endpoint
- Supports software controlled PHY register access
- Ready to use component for Qsys
- Meets Altera Design Assistant guidelines
- Optimized for use with Altera Nios II embedded processor
- Optimized LE count

Implementation Results

Supported Families	Resource Utilization	Performance (fmax) MHz	Memory Blocks
Cyclone III	2487 LE	250	4 M9Ks
Cyclone IV GX	2487 LE	250	4 M9Ks
Cyclone V	1098 ALM	240	4 M10Ks
Startix IV	1724 ALUT	490	4 M9Ks
Startix V	1069 ALM	500	4 M20Ks
Arria II	1729 ALUT	260	4 M9Ks
Arria V	1083.5 ALM	285	4 M10Ks

Supported Families	Resource Utilization	Performance (fmax) MHz	Memory Blocks
MAX 10	2464 LE	250	4 M9Ks

Deliverables

Contents	Eval	Full
OpenCore Plus Evaluation: One (1) month evaluation license at no cost	✓	
Full Version: One (1) Year development license with full version purchase for single project and single site. Other licensing schemes are also available.		✓
Demonstrations: 1) Performance Test (Streaming Bulk IN and Bulk OUT)	✓	✓
Time-limited (4 hours) SOF generation support	✓	
Full programming files generation support		✓
Reference Design for CoreCommander Development Board	✓	✓
USB 2.0 Host BFM simulation model for Altera Modelsim	✓	✓
Nios II Sample Applications (with C code): 1) Streaming	✓	✓
HAL Driver object code	✓	✓
Windows Reference Drivers (object code)	✓	✓
Software Library: 1) VC++	✓	✓
Utilities: 1) USBView	✓	✓
Documentation: 1) IP Core User Guide 2) Host BFM User Guide 3) Windows API User Guide 4) HAL API User Guide	✓	✓

Support

- IP integration support available with the purchase of full version
- Additional support on chargeable basis for a period of 3 months or more
- IP Core modification support available at additional cost

Verification

- IP Core has been tested by interfacing it with USB 2.0 PHY on SLS CoreCommander development board.
- USB20SF IP core's functionality is verified in ModelSim simulation software using test bench written in Verilog HDL.

Licensing

- **OpenCore Plus Evaluation**: 1 month evaluation license at no cost
- **Full**: 1 Year development license with full version purchase for single project and single site
- **Renewal**: OpenCore Plus Evaluation license update at discounted price

Contact info@slscorp.com for more information and sales @slscorp.com for placing an order.

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