ELTAN

eSPI POST Code Card

Features
(UEFI) BIOS debug code display
Port 80 and Port 81 display

Phoenix® BIOS POST code, Intel® FSP debug code, AMD firmware initialization code, UEFI debug code, Coreboot™ Open Source firmware debug code, etc.

Serial out of:
Port 80/81 code and also of Port 82/83
Byte display and Word display format

USB powered:
Display of power down POST code sequence, while power rails on target are switched off.

The Eltan POST Code Card for eSPI displays "Port 80h" and "Port 81h" (UEFI-) BIOS POST codes on 4x 7-segment display.

And (to enable logging of these POST codes) sends these HEX codes over a serial connection to a Host PC, which allows terminal software to record the complete Port 80/81/82/83 sequence.
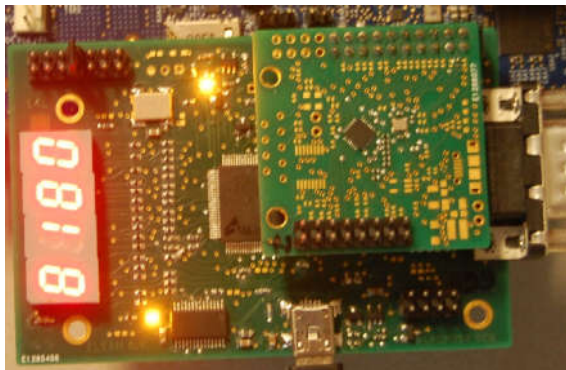
The eSPI interface signals are monitored, which enables to distinguish Byte and Word access, which is valuable POST code information.

Mechanical Interface:
The 2x10 way socket fits onto the standard "eSPI header" (0.1"pitch) located on the target main board.
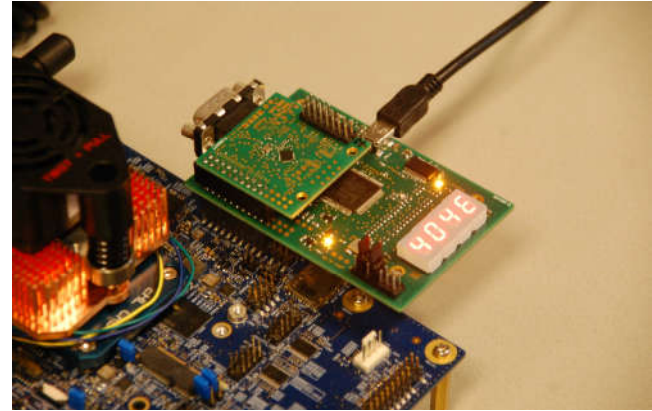
Applications
- BIOS firmware debugging x86 PC board
- PC computer repair tool
- Functional x86 board test-fixture tool

4 times a Byte to 80, 81, 82 and 83, and 2 times a Word to port 80 and 82 BIOS POST code example

eSPI Specification
The Eltan eSPI POST code card monitors the eSPI signals between the eSPI Master (the chipset) and an eSPI slave (BMC chip, eSPI embedded controller, or Super IO chip) on the main board. In case the main board does not have such eSPI slave chip then the eSPI POST Card with eSPI Slave is required.

eSPI Clock: up to 50 MHz
eSPI data width: Single I/O and Quad I/O
(GET- & SET_CONFIGURATION eSPI Spec. Commands)

Mechanical dimensions
Board size: 89 mm x 58 mm

Operating temperature
0 °C – 70 °C

Order information
- eSPI POST Card
- eSPI POST Card with eSPI Slave

Or contact ELTAN about your requirements

Jumper settings
- Rotate 4x 7 segment display to avoid reading upside down

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Datasheet revision:
8 October 2021