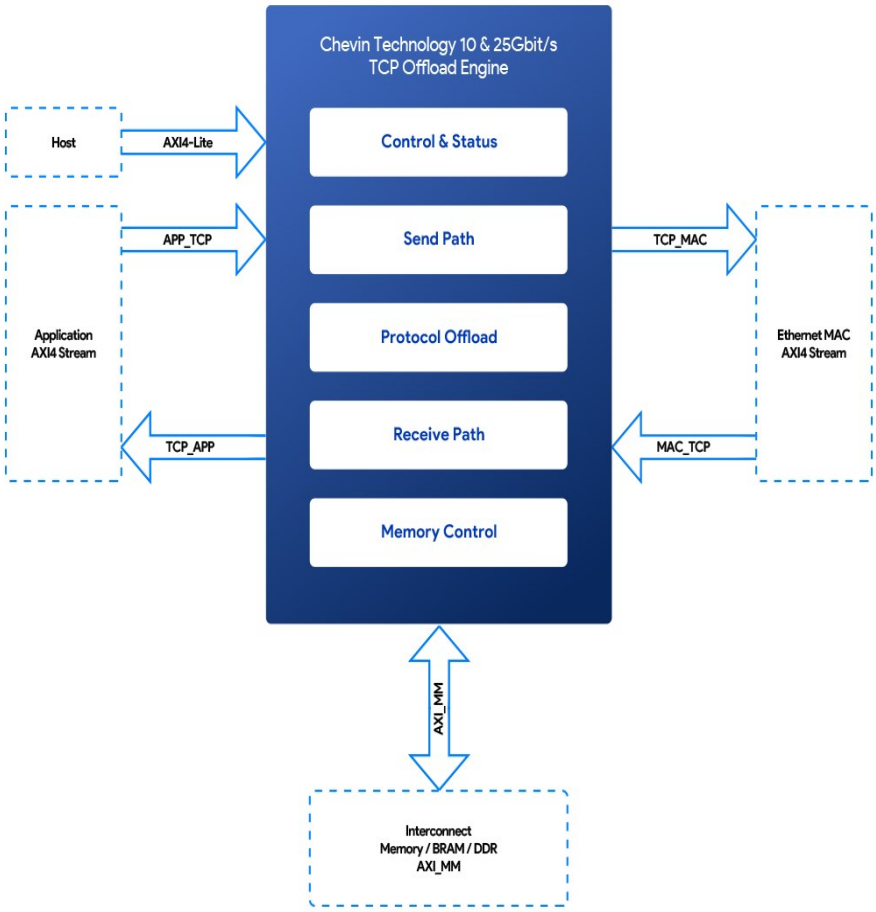
10G/25G TCP/IP Offload Engine

CT1008-TCPIP - Product Brief - Version 1.3 – January 2023

The TCP/IP (Transmission Control Protocol/ Internet Protocol) is an Ethernet IP core for FPGAs that incorporates both the transport and internet layer protocols to deliver reliable, end to end network communications using the internet or on private networks.

Chevin Technology's 10G/25G TCP/IP Offload Engine is an FPGA Synthesizable Ethernet TCP/IP server/client in a lean and fast, all-RTL solution. The TCP/IP Offload Engine provides a quick path to creating TCP enabled applications with a minimum of additional resources for network management at the FPGA side. The AXI4-Lite host interface permits control of the TCP's registers and statistics for connection and link monitoring, and is routable per session.

The TCP Offload Engine is highly configurable to optimize data exchange, power consumption and latency. The software driver allows users to easily manage features such as sending and receiving data to applications using DMAs (useful to implement higher level protocols); control routing and manage load balancing of the TCP to multiple applications; and to dynamically switch between AXI4 Streaming and AXI4 MM. By storing data and streaming from memory, the AXI4 Streaming and memory interface reduces power consumption by up to 2/3rds, as well as decreasing latency and complexity. The AXI4-Stream compliant user interface provides flow control, session identification and routing capabilities that offer seamless integration with system development and productivity tools such as Xilinx Vitis/Vivado and Intel Quartus/Platform Designer.



Key Features

· 1 to 256 simultaneous TCP/IP sessions
· Low latency, high throughput performance
· Server/Client, configurable per session
· Zero Copy—Dynamic Stream/ Memory Source and Destination switching
· Automatic, independent socket connection
· ARP—Cache & Table, Request & Reply
· ICMP - Ping Request & Reply
· Programmable per session receive/ congestion window
· AXI4_MM memory
· Configurable TX & RX buffer size: 1KB-1GB
· 64-bit AXI4 stream @ 156.25 MHz
· AXI4 MAC interface will connect to any Ethernet MAC, including Xilinx, Intel & Chevin
· AXI4 routing capability on all interfaces, per session, which allows for flexible routing options to multiple applications, MACs or other interfaces

Chevin Technology Ltd., The Bradfield Centre, 184 Cambridge Science Park, Milton Road, Cambridge, Cambridgeshire, CB4 0GA, UK
Telephone: +44 (0)1223 817009 Email: ip@chevintechnology.com www.chevintechnology.com

10G/25G TCP/IP Offload Engine

Integration in FPGA

The TCP IP core's flexibility provides a powerful way to configure some or all sessions during run-time. All sessions can be set to either accept connections as server, or initiate connections as a client. TCP port numbers can be automatically allocated by the software driver or selected by the user, and the TCP IP core can run as a concurrent or iterative server.

Chevin Technology's TCP offloads the TCP protocol using fast and efficient logic for checksum calculation, and is easily integrated alongside other protocols to provide an easy path for the development of TCP enabled FPGA applications. The User application side and MAC connect to the TCP IP core with an AXI4-Stream interface that is recognized by Xilinx and Intel FPGAs for easy integration and seamless connectivity. The TCP IP core can be configured to initiate (client) or accept (server) a TCP connection with a remote endpoint. Once a session is established, data can be reliably sent and received over the TCP protocol; taking care of checksum insertion/ checking, sockets and flow control at high, sustained data rates of 10 or 25 Gbit/s. The TCP core supports multiple, simultaneous connections, and handles opening and closing connections with no requirement for additional software support. Re-transmit is managed by a control layer within the TCP for fast, easy error recovery.

Chevin Technology's TCP IP Core also features our patent-pending Authentication Solution, which provides further design flexibility and cost efficiency, as clients have the option of adding extra features as required throughout the design cycle.

Chevin Technology offer flexible licensing terms as well as additional maintenance and engineering support packages for successful implementation.

Throughput & Latency Figures

TCP send/receive rate: 9.5 Gbps (1.2 GB/s); TX / RX– Latency < 1 us

Devices

Xilinx UltraScale; Ultrascale+; Zynq; 7 Series, Virtex, Kintex, Alveo

Intel Agilex; Stratix; Arria

FPGA Resource Figures

Xilinx Zynq ZCU102

Intel Agilex Bittware IA840F

Sessions	LUTs	BRAMs
1	32k	90
8	36k	92
32	40k	102

Deliverables

- *Encrypted compiled netlist*
- *Datasheet & User Guide*
- *Reference Designs/Examples*
- *Simulation Test bench*
- *Build scripts for Vivado, Quartus*
- *Software Driver*
- *Support for integration into FPGA*

Markets

- *Defence*
- *Scientific*
- *Aerospace*
- *Cyber security*
- *Medical*
- *Finance*
- *Telecoms*
- *Broadcast*

Applications

- *Artificial Intelligence*
- *Machine Learning*
- *Video Imaging*
- *Image/Signal Processing*
- *Internet Security Monitoring*
- *Data Storage & Capture Systems*
- *Trade Execution & monitoring*
- *HPC/ Big Data systems*
- *Data Mining*

Chevin Technology Ltd., The Bradfield Centre, 184 Cambridge Science Park, Milton Road, Cambridge, Cambridgeshire, CB4 0GA, UK

Telephone: +44 (0)1223 817009 Email: ip@chevintechnology.com www.chevintechnology.com