MAC/PCS for 10 &25 Gbit/s Ethernet

CT10**MAC/PCS - Product Brief - Version 1.3 – February 2023

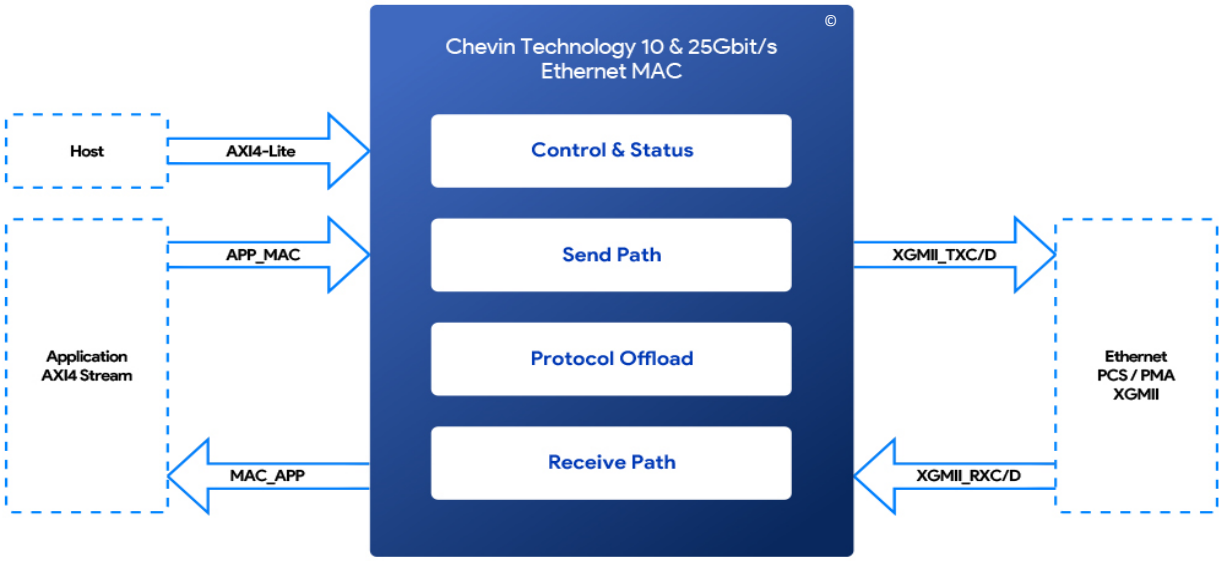
Chevin Technology's 10/25G MAC/PCS combines the MAC and PCS IP cores to obtain the lowest possible latency while simplifying the integration of 10/25Gbit/s Ethernet connectivity in Intel and Xilinx FPGAs. Low latency is achieved on the PCS block by using only the PMA function in FPGA Multi-Gigabit transceivers and moving into RTL all PCS functions to code that is optimized for 10GBASE-R. This allows the data to take the shortest, therefore the lowest, latency path to and from the wire. The MAC manages frame timing, CRC32 Checksum insertion and generation, and manages the lower layer fault handling and XGMII interface coding. Chevin Technology's MAC/PCS is XGMII compatible with a 64bit interface at 156.25/390.625MHz. A detailed statistics block provides a running count of frames sent and received with individual 64bit counters for different frame sizes, types and checksum errors. Achieve smoother, faster integration with the Chevin Technology reference design on Bittware IA-840f, IA-420f boards; AlphaData; ADM-PCIE-8V3, ADM-PCIE-9V3, Xilinx Virtex® UltraScale™ and UltraScale+™ development boards. Use standard software TCP/UDP tools when integrated with Chevin Technology's TCP/IP or UDP/IP cores.

Deliverables

- *Encrypted compiled netlist*
- *Datasheet & User Guide*
- *Reference Designs*
- *Simulation Test bench*
- *Build scripts for Vivado*
- *Software Driver*
- *Support for integration into FPGA*

Key Features

- *Designed to IEEE 802.3by 25GBASE-R; 802.3a 10GBASE-R*
- *10G MAC/PCS—Low Latency 153.8 ns packet Round Trip Time (RTT) in Virtex® UltraScale™ 5153 LUTs*
- *25G MAC/PCS—Low Latency 128 ns packet Round Trip Time (RTT) in Virtex® UltraScale™ 7930 LUTs*
- *Integrated FCS CRC32 check/generate*
- *Flow Control option with Pause packets*
- *Deficit Idle Count / Programmable IFG – Minimize IFG*
- *Cut-through mode for minimum latency*
- *Store-and-forward for minimum app load*
- *Fault Management, BER monitoring*
- *Statistics counters for frames and bytes sent/*



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Integration in FPGA

The reference design includes a top level wrapper for the IP and includes build scripts and constraints. A simple host interface makes it possible to read and write registers for monitoring purposes, and can be used to speed up integration work.
The 64bit XGMII interface connects directly to any XGMII compatible PCS, preferably utilizing Virtex® UltraScale™ devices that are 10/25Gbit capable. This combination provides the lowest possible latency, power, board size and cost, and the best overall performance. The application side connects directly to user logic which can be user logic FIFOs to AXI4 standard interfaces or shared via an arbiter to other stack layers such as TCP/IP, UDP/IP, ICMP and ARP, also supplied by Chevin Technology, for a more integrated FPGA solution.

Throughput & Latency Figures

Round trip delay (Ultrascale)
MAC(in) -> SFP28 (wire) -> MAC(out) 10G - 153.8ns, 25G - 128 ns

FPGA Resource Figures

10G PCS/PMA 3024 LUTs, 25G PCS/PMA 5107 LUTs

Markets

- *Defense*
- *Scientific*
- *Aerospace*
- *Cyber security*
- *Medical*
- *Finance*
- *Telecoms*
- *Broadcast*
- *Data Centre*

Applications

- *Artificial Intelligence*
- *Machine Learning*
- *Video Imaging*
- *Image/Signal Processing*
- *Internet Security Monitoring*
- *Data Storage & Capture Systems*
- *Trade Execution & monitoring*
- *HPC/ Big Data systems*
- *Data Mining*

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