TEGUAR®
Corporation

TB-5545-MVS Series

Mini-ITX, 7th Generation, Intel Core i3/i5/i7 Processor Machine Vision Fanless Box PC

User Manual

Warning!_____

This equipment will generate, use and radiate radio frequency energy and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to FCC Rules, which is designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user with its own expense will be required to take whatever measures may be required to correct the interference.

Electric Shock Hazard – Do not operate the machine with its back cover removed. There are dangerous high voltages inside.

Packing List

Accessories (as ticked) included in this package are:
☐ Adaptor ☐ Driver & manual CD disc ☐ Other._____(please specify)

Safety Precautions

Follow the messages below to prevent your systems from damage:

- Avoid your system from static electricity on all occasions.

- Prevent electric shock. Don‘t touch any components of this card when the card is power-on. Always disconnect power when the system is not in use.

- Disconnect power when you change any hardware devices. For instance, when you connect a jumper or install any cards, a surge of power may damage the electronic components or the whole system.

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- Machine Vision Application System
- Intel 7th Gen. Core i3/i5/i7 Processor
- Fanless Design
- 2 x 260-pin DDR4 SO-DIMM Memory
- 9~36V DC Wide-ranging Power input

1.2 Specifications

	TB-5545-MVS Series
System	
CPU	Intel 7th Gen. Core i3/i5/i7 Processor
Chipset	SoC
Memory	2 x 260-pin DDR4 SO-DIMM memory, up to 32GB
Outside IO Port	
Front I/O Ports	4 x USB 3.0 type A, 2 x USB 2.0 type A via TX-F77, 1 x internal USB dongle 2 x GbE LAN RJ-45 1 x RS-232/422/485 DB-9, Default RS-232, COM1 1 x RS-232 DB-9, COM2 1 x RS-422/485 for COM3, default RS-485 1 x RS-232 for COM4 1 x Audio line-out 1 x Mic-in 1 x VGA 1 x 8-bit GPIO 4 x in, 4 x out via TX-F77 1 x 2-pin power switch connector 1 x Power button with light via TX-F77
Storage Space	
Storage	2 x 2.5” SATA3 HDD/SSD (Easy-swappable HDD tray)
Expansion	
Expansion Slot	TB-5545-MVS: N/A
	TB-5545-MVS x2 expansion: 2 x PCI/PCIe slots

	TB-5545-MVS-x4 expansion: 4 x PCI/PCIe slots		
Power			
Power Input	9~36V DC		
Mechanical			
Construction	Plating Titanium Gray Aluminum Heatsink and Black Steel Chassis		
Mounting	Din Rail back side(option)/Wall Mount(option)		
Dimensions	220 x 149 x 68 mm		
Net Weight	TB-5545-MVS:3.1Kg	x2 expansion:3.7Kg	x4 expansion:4.1Kg
Environmental			
Operating Temperature	-20~60℃(for i3/i5 model)	-20~50℃(for i7 model)	
Storage Temperature	-40~85℃		
Storage Humidity	10 to 90% @ 40℃, non-condensing		
Certification	CE / FCC Class A		
Operating System Support	Microsoft® Win10 IoT, Windows 7, Linux Kernel 4.15 (Ubuntu 16.04.4)		

1.3 Dimensions

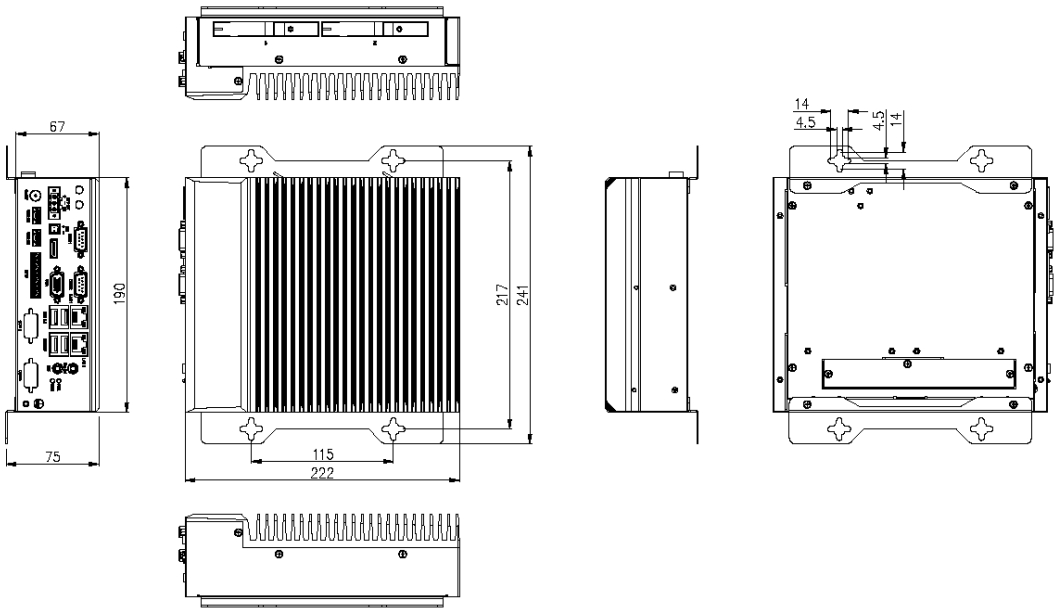


Figure 1.1: Dimension of TB-5545-MVS

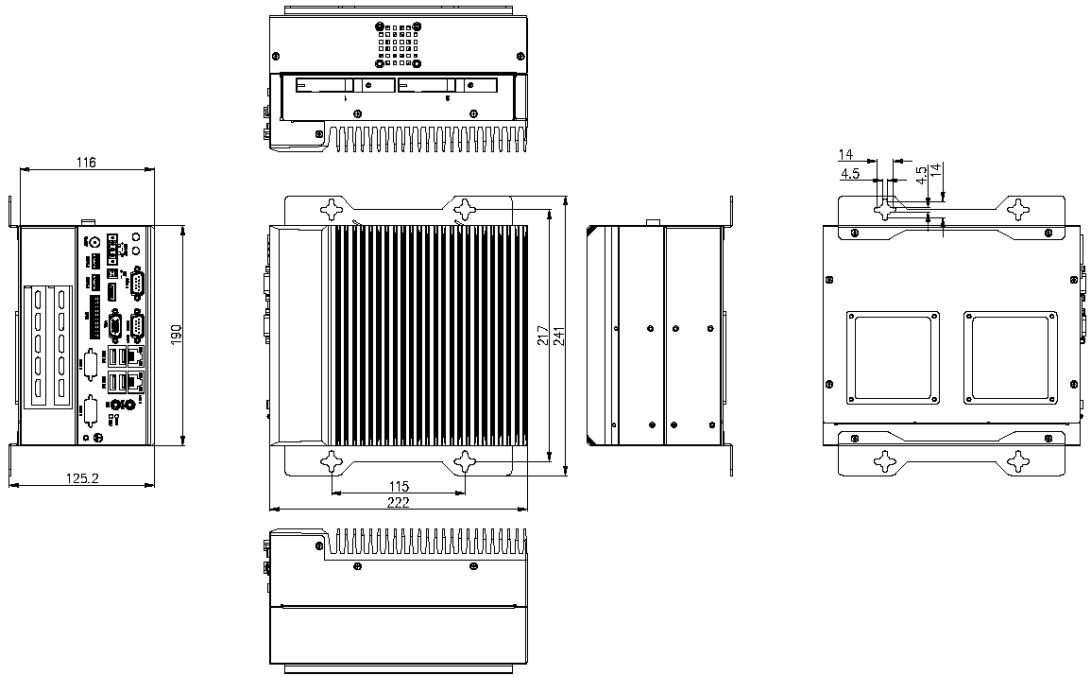


Figure 1.2: Dimension of TB-5545-MVS x2 expansion

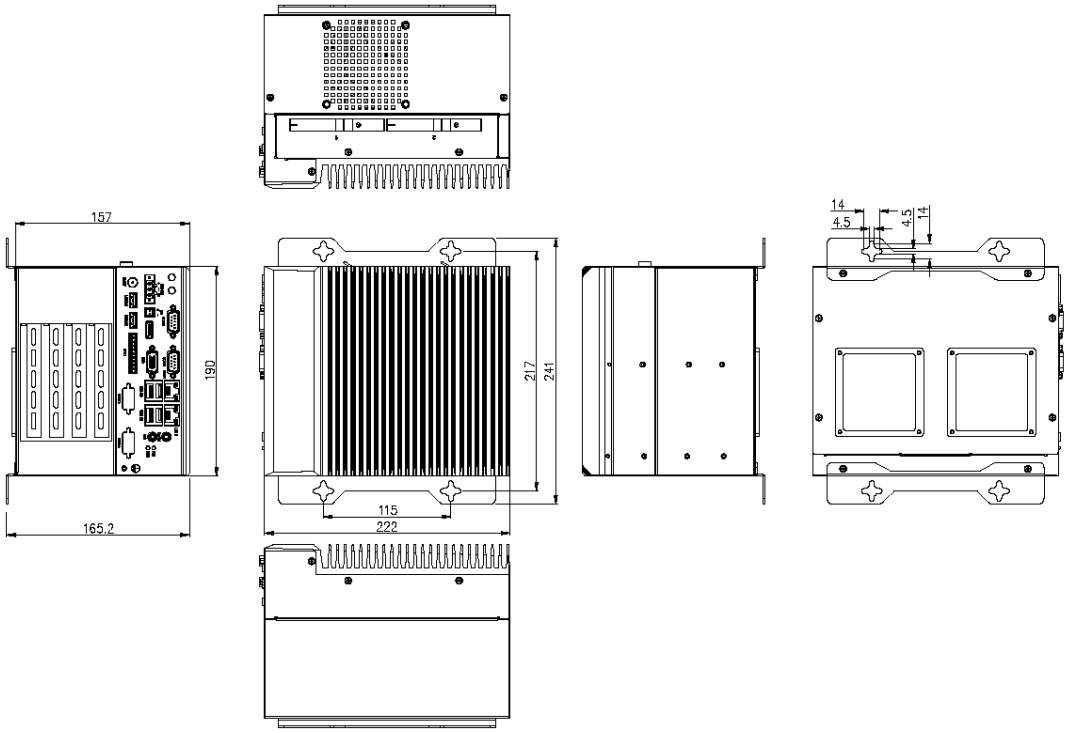


Figure 1.3: Dimension of TB-5545-MVS x4 expansion

1.4 Brief Description of TB-5545-MVS Series

TB-5545-MVS series are fanless-design high-efficiency BOX PC, powered by Intel 7th Generation Core i3/i5/i7 processor and supports 2 x 260-pin DDR3 SO-DIMM up to 32GB memory. They come with 4 x USB 3.0 Type A, 2 x USB 2.0 Type A, 2 x LAN, 1 x VGA, 4 x COM ports(with 2 reserved), 1 x audio line-out, and 1 x power button. They support 2 x 2.5" SATA3 HDD space which is easy accessible design and 9~36V DC wide-ranging power input. The models have up to 4 x PCI/PCIe slot for expansion. The models are plating titanium gray aluminum heatsink and black steel chassis design, and can be din rail-mounted and wall-mounted. The TB-5545-MVS series work well with our other products and they can provide an absolute easy way to perform control maintenance.

Figure 1.4: Appearance of TB-5545-MVS

Figure 1.5: Appearance of TB-5545-MVS x2 expansion

Figure 1.6: Appearance of TB-5545-MVS x4 expansion

Chapter 2 Hardware

2.1 Motherboard Introduction

TB-5545-MVS series is a non-standard industrial motherboard developed on the basis of Intel H170, which provides abundant peripheral interfaces to meet the needs of different customers. Also, it features dual GbE ports, 6-COM ports and two mPCIE configuration. To satisfy the special needs of high-end customers, TB-5545-MVS series is designed with 120-pin PCIe x 16 socket extension interface. The product is widely used in various sectors of industrial control.

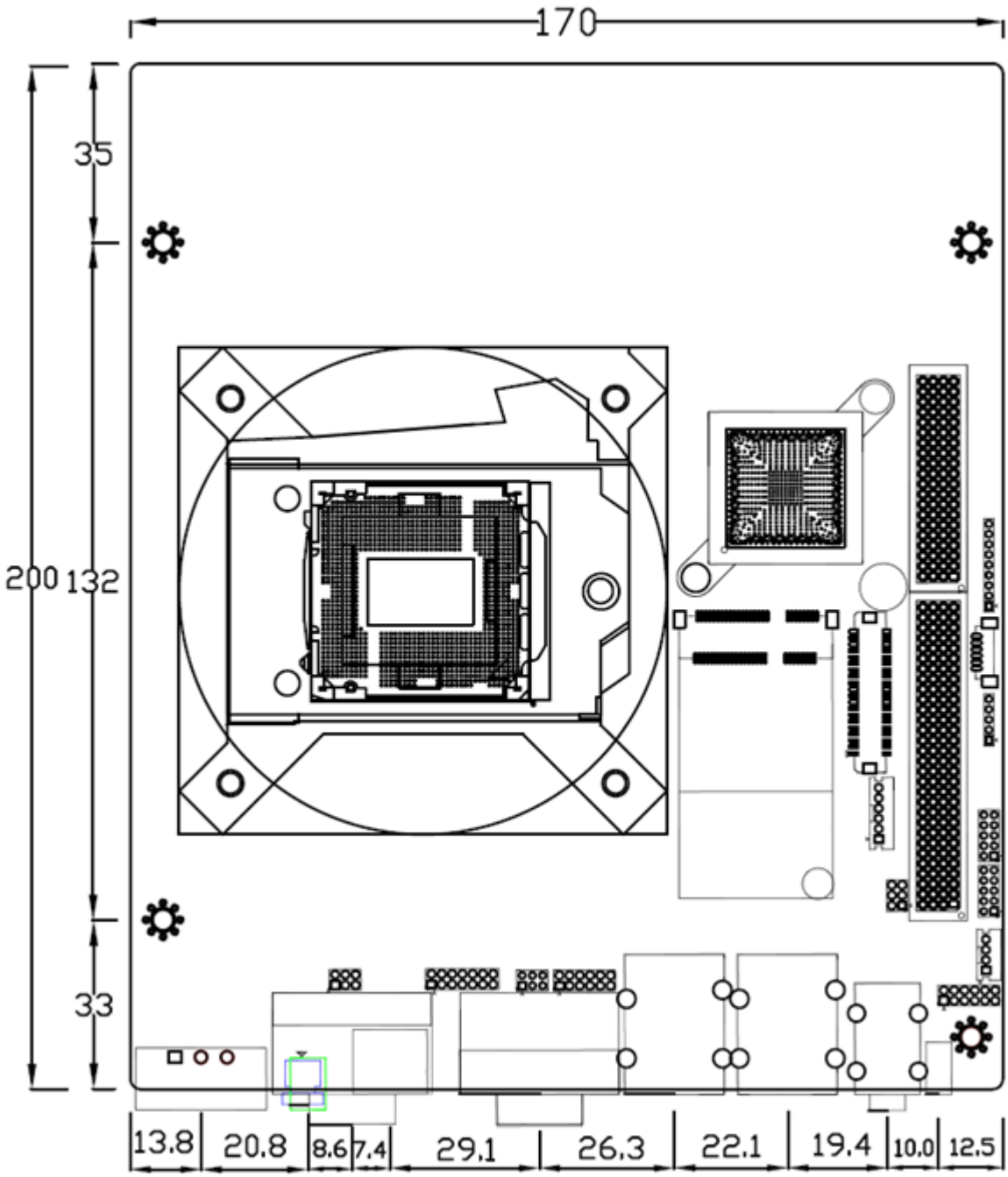
2.2 Specifications

Specifications	
Board Size	200mm x 170mm x 1.6mm
CPU Socket	LGA 1151 Socket
CPU Support	Intel 6th /7th Core i3/i5/i7 Processor (up to 35W) Intel® Core™ I3-6100TE, 2.70GHz 35W Intel® Core™ I5-6500TE, 2.30GHz (up to 3.30 GHz) 35W Intel® Core™ I7-6700TE, 2.40GHz (up to 3.40 GHz) 35W Intel Pentium Processor G4400TE 2.30GHz 35W Intel Celeron Processor G3900TE 2.30GHz 35W Intel® Core™ I3-7101TE 3.40GHz 35W Intel® Core™ I5-7500T 2.70GHz (up to 3.30GHz) 35W Intel® Core™ I7-7700T 2.90GHz (up to 3.80GHz) 35W Intel Celeron Processor G3930TE 2.70GHz 35W
Chipset	Intel H170
Memory Support	2 x SO-DIMM (260pins), up to 32GB DDR4 1866/2133 MHz FSB(6Gen) 2 x SO-DIMM (260pins), up to 32GB DDR4 2133/2400 MHz FSB(7Gen)
Graphics	Intel® HD Graphics 530(I3-6100TE/I5-6500TE/I7-6700TE) Intel® HD Graphics 510(G4400TE/G3900TE) Intel® HD Graphics 630(I3-7101TE/I5-7500T/I7-7700T) Intel® HD Graphics 610(G3930TE)
Display Mode	1 x HDMI via HDMI Port

	1 x LVDS (18/24-bit dual LVDS) (option) 1 x VGA via DB15 or 2x6 pin header 1 x DVI-I via pin header
Support Resolution	Up to 4096 x 2304 for HDMI Up to 1920 x 1200 for LVDS (option) Up to 2560 x 1600 for DVI-I Up to 1920 x 1200 for VGA
Three Display	HDMI + DVI-I + VGA1/CRT1 HDMI + DVI-I + LVDS (option) HDMI + LVDS + VGA1/CRT1 (option) DVI-I + LVDS + VGA1/CRT1 (option)
Super I/O	Nuvoton NCT6106D
BIOS	AMI/UEFI BIOS
Storage	3 x SATA3.0 Connector (SATA1/SATA2/SATA3)(Bottom side) 1 x MSATA Connector 1 x mini PCI-express slot(MPCIE1, option)
Ethernet	2 x PCIe Gbe LAN, RJ45 via Intel I210AT
USB	4 x USB 3.0/2.0 stack ports for external (USB 3.0: USB3-1/USB3-2/USB3-3/USB3-4) (USB 2.0: USB2-1/USB2-2/USB2-3/USB2-4) 3 x USB 2.0 Pin header for MIO1 (USB9/USB12/USB13) 4 x USB 2.0 Pin header for MIO2 (USB7/ USB8/USB10/USB11) 1 x USB 2.0 internal for MPCIE1 (USB14) 1 x USB 2.0 internal for MPCIE2 (USB9)
Serial	1 x RS232/RS422/RS485 port, DB9 connector for external (COM1) Pin 9 w/5V/12V/Ring select 1 x RS232 port, DB9 connector for external (COM2) Pin 9 w/5V/12V/Ring select 1 x RS422/485 select header for internal MIO1 (COM3) 1 x RS232 select header for internal MIO1 (COM4) 1 x RS232 header for internal (COM5) 1 x RS232 header for internal (COM6), pin9 w/5V/12V/Ring select
Digital I/O	8-bit digital I/O by pin header (MIO2) 4-bit digital input 4-bit digital output
Battery	Support CR2477 Li battery by 2-pin header (1000mAh)

Audio	Support Audio via Realtek ALC269Q-VC HD audio codec(option) Support Line-out, Line-in, MIC-in by JACK (AUDIO1) Line-in/Line-out/MIC by 2x6-pin header(F-AUDIO1) Support a stereo Class-D Speaker Amplifier with 2 watt per channel output power, by 1 x 4-pin header (SPK1)
Keyboard /Mouse	1 x PS2 keyboard/mouse by MIO2 1 x PS/2 keyboard 1 x PS/2 mouse
Expansion Bus	5 x PCI-express x1 extend by 4x20 pin socket(PCIE_4x1) 1 x PCI-express x16 extend by 4x30 pin socket(PCIE_16x1, GEN2) 1 x mini-PCI-express slot (MPCIE1, option) 1 x mini-PCI-express slot (MPCIE2) 1 x CRT 2x5 Pin header (VGA1)
Power Management	DC 9~36V in via 3-pin Connector (input) 1 x DC 12V out via 2-pin Connector (output, option)
Switches and LED Indicators	Power on/off switch by MIO1 and MIO2 Power LED status by MIO1 and MIO2 HDD LED status by MIO2 Reset switch by MIO2
External I/O Port	2 x COM Ports 4 x USB 3.0 Ports(stack) 2 x RJ45 GbE LAN Ports 1 x HDMI interface 1 x CRT interface 1 x Audio Port(Mic-in, Line in, Line out)
SIM	1 x SIM Card holder, 1 x 6-pin Wafer by SIM1(option)
TPM	Infineon's Trusted Platform Module(TPM2.0, option)
Temperature	Operating: -20℃ to 70℃ Storage: -40℃ to 85℃
Humidity	10% - 90%, non-condensing, operating
Power Consumption	24V/2A(Intel I3-6100TE 2.30GHz Processor with 16GB DDR4/SSD)
EMI/EMS	Meet CE/FCC Part15 class A RoHS

2.3 Motherboard Dimension



(units :mm)

Figure 2.1: Motherboard TB-5545-MVS series Dimensions

2.4 Jumpers and Connectors Location

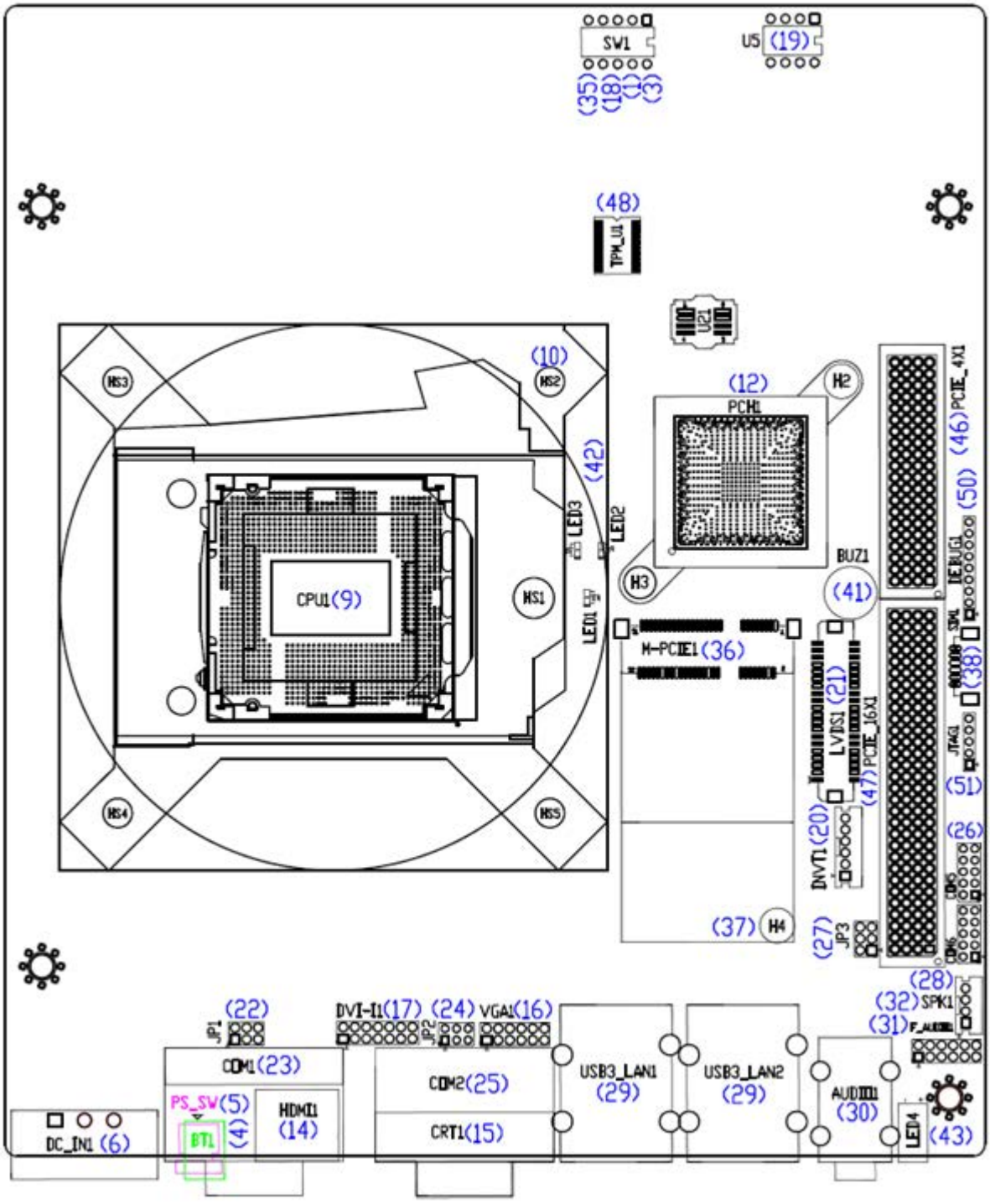


Figure 2.2: Jumpers and Connectors Location- Board Top

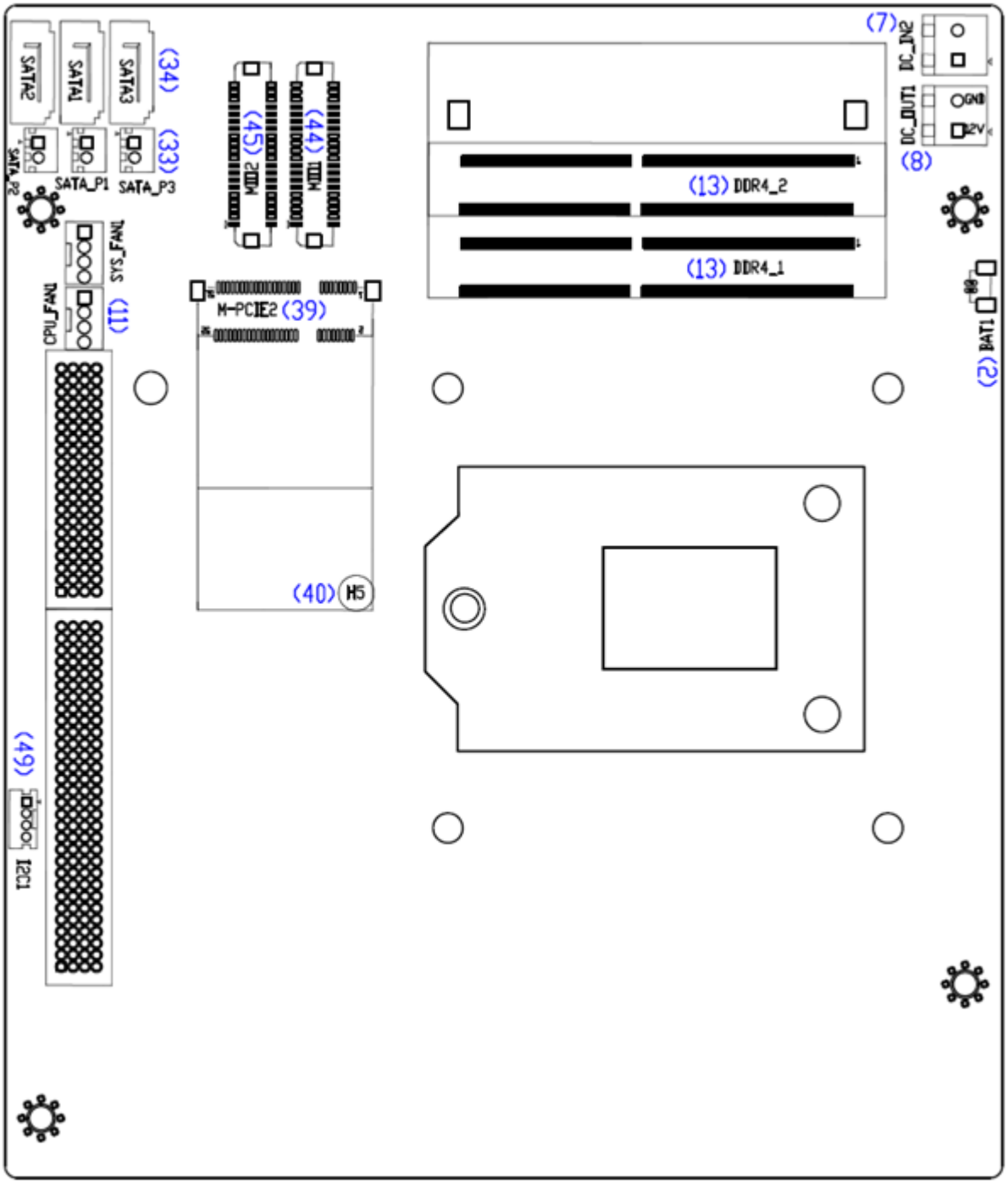


Figure 2.3: Jumpers and Connectors Location- Board Bottom

2.5 Jumpers Setting and Connectors

1. SW1-2:

CMOS clear switch, CMOS clear operation will permanently reset old BIOS settings to factory defaults.

SW1	CMOS
Pin2 OFF	NORMAL (Default)
Pin2 ON	Clear CMOS

Procedures of CMOS clear:

a) Turn off the system and unplug the power cord from the power outlet.

b) To clear the CMOS settings, use the switch to Pin2 on for about 3 seconds then move the switch Pin2 off.

c) Power on the system again.

d) When entering the POST screen, press the <DEL> key to enter CMOS Setup Utility to load optimal defaults.

e) After the above operations, save changes and exit BIOS Setup.

2. BAT1:

(1.25mm Pitch 1x2 wafer Pin Header) 3.0V Li Battery is embedded to provide power for CMOS.

Pin#	Signal Name
Pin1	Ground
Pin2	VCC_RTC

3. SW1-1:

Switch, DC Power input setting, Power on/off button and Auto Power on switch setting.

SW1	Function（DC input /DC_IN1）
Pin1 ON	**Auto Power on (Default)**
Pin1 OFF	Power on/Off button (option)

4. BT1 (option):

(2.0mm Pitch 1x2 Wafer Pin Header) Power on/off, is use to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup& shutdown or awaken the system from sleep state.

Model	BT1
TB-5545-MVS	●
TB-5545-MVS	X

5. PS_SW (option):

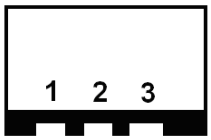
PW_SW: POWER on/off Button, is used to connect power switch button. The two pins are disconnected under normal condition. You may short it to realize system startup& shutdown or awaken the system from sleep state.

PWR LED: POWER LED status

Model	PS_SW
TB-5545-MVS	X
TB-5545-MVS s	●

6. DC_IN1:

(5.08mm Pitch 1x3 Pin Connector), DC9~36V system power input connector. Maximum power consumption of the whole machine is not more than 150 watts. If it is used in visual system of light control, please use 24V/7.5A power adapter.



Pin#	Power Input（DC_IN1）
Pin1	DC+9V~36V
Pin2	Ground
Pin3	PG

Application	Power Adapter
Vision/ Light Control （DC24V）	**+DC24V input (Recommend:24V/6.25A)**
Box PC	DC+9V~36V input

7. DC_IN2 (option):

(5.08mm Pitch 1x2 Pin Connector), DC9~36V System power input connector. DC_IN2 is directly connected to DC_IN1. The input power supply voltage is same as the output power supply voltage.

Pin#	Power Input（DC_IN2）
Pin1	DC+9V~36V
Pin2	Ground

Model	DC_IN2 (Reserve)
TB-5545-MVS	N/A
TB-5545-MVS s	N/A

8. DC_OUT1 (option):

(5.08mm Pitch 1x2 Pin Connector), DC12V System power output connector.

Pin#	Power output
Pin1	DC+12V
Pin2	Ground

Model	DC_OUT1 (Reserve)
TB-5545-MVS	N/A
TB-5545-MVS s	N/A

Note:

DC_OUT1 Output current of the connector must not be above 5A.

9. CPU1:

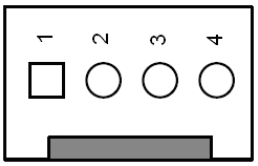
(LGA1151 Socket), used to install Intel 6th /7th i3/i5/i7 CPU.

10. HS2/HS3/HS4/HS5 (CPU SCREW HOLES):

4x CPU FAN SCREW HOLES to fix CPU cooler assemble.

11. CPU_FAN1/SYS_FAN1:

(2.54mm Pitch 1x4 Pin Header), Fan connector, cooling fans can be directly connected to use.



Pin#	Signal Name	CPU_FAN1	SYS_FAN1
1	Ground	●	●
2	VCC	●	●
3	CPU_FANTACH	●	●
4	CPU_FANPWM	●	●
Active Trip Point Fan Speed		CPU_FAN1	SYS_FAN1
BIOS CMOS Setup		X	X
BIOS CMOS Setup (option)		●	●

Note:

Output power of cooling fan must be limited under 5W.

12. PCH1:

(BGA, Package Size: 23x24mm) Intel H170 Chipset.

Model	PCH1（Chipset）
TB-5545-MVS	Intel H170
TB-5545-MVS s	Intel H170

13. DDR4_1/DDR4_2:

(SO-DIMM 260Pin socket), DDR4 memory socket, is located at top of the board and supports 260Pin 1.2V DDR4 SO-DIMM memory module up to 32GB.

CPU	Memory Types（FSB）
I3-6100TE I5-6500TE I7-6700TE G4400TE G3900TE	1866/2133MHz
G3930TE	2133MHz

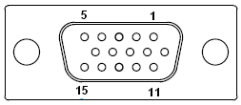
I3-7101TE	2400MHz
I5-7500T I7-7700T	2133/2400MHz

14. HDMI1:

(HDMI 19P Connector) High Definition Multimedia Interface connector, supports version HDMI1.4.

15. CRT1:

(CRT Connector DB15), Video Graphic Array Port, provide high quality video output. **CRT1 and VGA1 are not able to work at the same time.**



16. VGA1 (option):

(CRT 2.0mm Pitch 2x6 Pin Header), Video Graphic Array Port, provide 2x6 Pin cable to VGA port. The IT6515FN is a high-performance single-chip Display Port to VGA converter. **CRT1 and VGA1 are not able to work at the same time.**

Signal Name	Pin#	Pin#	Signal Name
CRT_RED	1	2	Ground
CRT_GREEN	3	4	Ground
CRT_BLUE	5	6	Ground
CRT_H_SYNC	7	8	CRT_DDCDATA
CRT_V_SYNC	9	10	CRT_DDCCLK
Ground	11	12	Ground

17. DVI-I1:

(DVI-I 2.0mm Pitch 2x7 Pin Header), Digital Visual Interface integrated connector.

Signal Name	Pin#	Pin#	Signal Name
DVI3_D2+	1	2	DVI3_D2-
DVI3_D1+	3	4	DVI3_D1-
DVI3_D0+	5	6	DVI3_D0-

DVI3_CLK+	7	8	DVI3_CLK-
DVI3_DDCCLK	9	10	DVI3_DDCDATA
Ground	11	12	Ground
5V_DVI	13	14	DVI3_HPDET

18. SW1-3/SW1-4 (option):

SW1	Function
Pin3 on	Single Channel LVDS
Pin3 off	**Dual Channel LVDS**
Pin4 on	**24bit LVDS**
Pin4 off	18bit LVDS

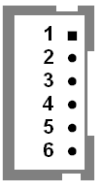
19. U5 (option):

AT24C02-DIP8, The EEPROM IC (U5) is the set of LVDS resolution. If you need other resolution settings, please upgrade U5 data.

Model	LVDS resolution
TB-5545-MVS Series	1280x1024 (Default)
	800x480 (option)
	800x600 (option)
	1024x768 (option)
	1920x1080 (option)
	……

20. INVT1 (option):

(2.0mm Pitch 1x6 wafer Pin Header) Backlight controller connector for LVDS.



Pin#	Signal Name
1	+DC12V_S0
2	+DC12V_S0
3	Ground

4	Ground
5	BKLT_EN_OUT
6	BKLT_CTRL

21. LVDS1:

(1.25mm Pitch 2x20 Connector, DF13-40P) 18/24-bit LVDS output connector. Fully supported by Parad PS8625 (DDI1 to LVDS), the interface features dual channel 24-bit output. Low Voltage Differential Signaling, a high speed, low power data transmission standard used for display connections to LCD panels.

Use SW1-3/SW1-4 selection switch to configure the settings. Please refer to section 18 for detailed information.

Signal Name	Pin#	Pin#	Signal Name
VDD5	2	1	VDD5
Ground	4	3	Ground
VDD3	6	5	VDD3
LB_D0_N	8	7	LA_D0_N
LB_D0_P	10	9	LA_D0_P
Ground	12	11	Ground
LB_D1_N	14	13	LA_D1_N
LB_D1_P	16	15	LA_D1_P
Ground	18	17	Ground
LB_D2_N	20	19	LA_D2_N
LB_D2_P	22	21	LA_D2_P
Ground	24	23	Ground
LB_CLK_N	26	25	LA_CLK_N
LB_CLK_P	28	27	LA_CLK_P
Ground	30	29	Ground
LVDS_DDC_DATA	32	31	LVDS_DDC_CLK
Ground	34	33	Ground
LB_D3_N	36	35	LA_D3_N
LB_D3_P	38	37	LA_D3_P
NC	40	39	NC

Model	U5	INVT1	LVDS1
TEG-M8172HB R1.00	N/A	N/A	N/A
TEG-M8172HB-S R1.00	N/A	N/A	N/A

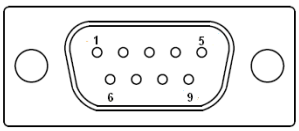
22. JP1:

(2.0mm Pitch 2x3 Pin Header), COM1 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM1 port.

JP1 Pin#	Function
Close 1-2	**COM1 RI (Ring Indicator) (default)**
Close 3-4	COM1 Pin9: DC+5V (option)
Close 5-6	COM1 Pin9: DC+12V (option)

23. COM1

(Type DB9M), Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



RS232 (Default)	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP1 select Setting (RI/5V/12V)**

RS422 (option)	
Pin#	Signal Name
1	422_TX-
2	422_TX+
3	422_RX+
4	422_RX-
5	Ground
6	NC
7	NC
8	NC

9	NC

RS485 (option)	
Pin#	Signal Name
1	485-
2	485+
3	NC
4	NC
5	Ground
6	NC
7	NC
8	NC
9	NC

BIOS/Serial Port 1 Configuration/F75111 COM1 Config:

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

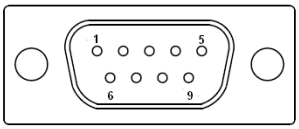
24. JP2:

(2.0mm Pitch 2x3 Pin Header), COM2 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM2 port.

JP2 Pin#	Function
Close 1-2	**COM2 RI (Ring Indicator) (default)**
Close 3-4	COM2 Pin9: DC+5V (option)
Close 5-6	COM2 Pin9: DC+12V (option)

25. COM2:

(Type DB9M), Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)

4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP2 select Setting (RI/5V/12V)**

26. COM5:

(2.0mm Pitch 2x5 Pin Header), COM5 Port, standard RS232 ports are provided. It is directly used via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
RI	9	10	NC

27. JP3:

(2.0mm Pitch 2x3 Pin Header), COM6 jumper setting, pin1~6 are used to select signal out of pin 9 of COM6 port.

JP3 Pin#	Function
Close 1-2	**COM6 Pin9 RI (Ring Indicator) (default)**
Close 3-4	COM6 Pin9=+5V/1A (option)
Close 5-6	COM6 Pin9=+12V/1A (option)

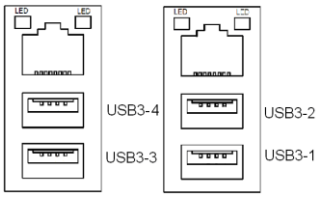
28. COM6:

(2.0mm Pitch 2x5 Pin Header), COM6 Port, standard RS232 ports are provided. It is directly used via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
JP3 select Setting (RI/5V/12V)	9	10	NC

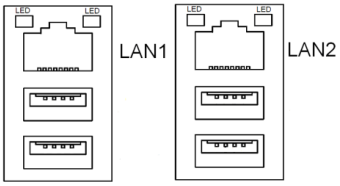
29. USB3_LAN1/USB3_LAN2:

USB3-1/USB3-2/USB3-3/USB3-4: (Double stack USB type A), Rear USB connector, provides up to 4x USB3.0 ports. USB 3.0 allows data transfer up to 5.0 Gb/s, supports USB 2.0 and full-speed and low-speed signaling.



Each USB Type A Receptacle (2 Ports) current value is limited in 2.0A.
If the external USB device current exceeds 2.0A, please separate connectors into different Receptacle.

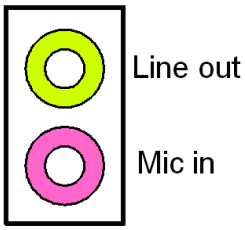
LAN1/LAN2: (RJ45 Connector), Rear LAN Port provides two standard 10/100/1000 RJ-45 Ethernet ports here. This port uses Intel I210AT chipset.



Model	U28/U36
TEG-M8172HB R1.00	Intel I210AT
TEG-M8172HB-S R1.00	Intel I210AT

30. AUDIO1:

(Diameter 3.5mm Two-stack jack), High Definition Audio Port, an onboard Realtek ALC269Q-VC codec is used to provide high quality audio I/O ports.



31. F_AUDIO1:

(2.0mm Pitch 2x6 Pin Header), Front Audio, an onboard Realtek ALC269Q-VC codec is used to provide high-quality audio I/O ports. Line Out can be connected to headphone or amplifier. Line In is used for the connection of external audio source via a Line in cable. MIC is the port for microphone input audio.

Signal Name	Pin#	Pin#	Signal Name
+5V	1	2	GND_AUD
LINE-OUT-L	3	4	LINE-OUT-R
HPOUT_JD	5	6	LINE_IN_JD
LINE-IN-L	7	8	LINE-IN-R
MIC-IN-L	9	10	MIC-IN-R
GND_AUD	11	12	MIC1_JD

32. SPK1:

(2.0mm Pitch 1x4 Wafer Pin Header) Support a stereo Class-D Speaker Amplifier with 2 watt per channel output power.

Pin#	Signal Name
1	SPK_OUTL_P
2	SPK_OUTL_N
3	SPK_OUTR_N
4	SPK_OUTR_P

33. SATA_P1/SATA_P2/SATA_P3:

(2.5mm Pitch 1x2 Wafer Pin Header) Two onboard 5V output connectors are reserved to provide power for SATA devices.

Pin#	Signal Name
1	+DC5V_S0
2	Ground


Note:

Output current of the connector must not be above 1A.

34. SATA1/SATA2/SATA3:

(SATA 7P) 3 x SATA Connectors are provided, SATA1/SATA2/SATA3 transfer speedup to 6.0Gb/s.

RAID controller supports RAID0/RAID1/RAID5.

35. SW1-5:

(Switch) SATA or PCIE setting

SW1	M-PCIE (52Pin)
Pin5 on	PCIE7 Signal
Pin5 off	SATA4 Signal

36. M-PCIE1:

(Socket 52 Pin) Mini PCIE socket, is located at the top of the board, supports mini PCIe devices with USB2.0, SIM, SMBUS and PCIe/MSATA signal. MPCIe card size is 30 x 50.95mm.

Function	Support	Remarks
Mini PCIe (PCIe7)	●	(SW1-5:off)
Mini SATA	○	Option(SW1-5:on)
LPC bus	●	
SMbus	●	
SIM	●	
USB2.0 (USB14)	●	

37. H4:

M-PCIE1 SCREW HOLES, H4 for M-PCIE1 card (30 x 50.95mm) assemble.

38. SIM1:

(2.0mm Pitch 1x6 Pin Wafer Header) Support SIM Card devices.

Pin#	Signal Name
1	SIM_VCC
2	Ground
3	SIM_RST
4	NC
5	SIM_CLK
6	SIM_IO

39. M-PCIE2:

(Socket 52 Pin) Mini PCIe socket, is located at the bottom, and supports mini PCIe devices with USB2.0, SMBUS, and PCIe signal. MPCIe card size is 30 x 50.95mm.

Function	Support	Remarks
Mini PCIe (PCIe4)	●	
SMbus	●	
USB2.0 (USB19)	●	

40. H5:

M-PCIE2 SCREW HOLES, H5 for M-PCIE2 card (30 x 50.95mm) assemble.

41. BUZ1:

Onboard Buzzer

42. LED1/LED2/LED3:

LED1 STATUS: Green LED for M/B Power status.

LED2 STATUS: Green LED for M/B Standby Power Good status.

LED3 STATUS: Green LED for CPU Power status.

43. LED4:

Green LED for Motherboard Standby Power good status.

Yellow LED for HDD status.

44. MIO1:

(DF13-40P Connector) Use to expand output connector with one RS232 port, one RS422 or RS485 ports, three USB ports, one power LED and one power button via a dedicated cable connects to TX-F23 MIO1.

Function	Signal Name	Pin#		Signal Name	Function
COM3 (RS422/RS485)	485+/422TX+	2	1	422_RX+	COM3(RS422)
	485-/422TX-	4	3	422_RX-	
WLAN LED	3P3V_S0	6	5	Ground	
	WLAN_LED-	8	7	NC	
	5V_S5	10	9	5V_S5	
COM4(RS232)	RXD4	12	11	DCD4-	COM4(RS232)
	DTR4-	14	13	TXD4	
	DSR4-	16	15	Ground	
	CTS4-	18	17	RTS4-	
	5V_S5	20	19	RI4-	
USB2.0(USB13)	5V_USB10/11	22	21	5V_S5	
	USB13_N	24	23	USB12_N	USB2.0(USB12)
	USB13_P	26	25	USB12_P	
	Ground	28	27	Ground	
	Ground	30	29	Ground	
Power LED	Power LED+	32	31	5V_USB10/11	USB2.0(USB9)
	Power LED-	34	33	USB9_N	
Power Button	MIO_PSON-	36	35	USB9_P	
	Ground	38	37	Ground	
Power Auto on	AUTO_PSON-	40	39	NC	

BIOS Setup:
Advanced/NCT6106D Super IO Configuration/Serial Port 3 Configuration:
[RS-485 Mode]
[RS-422 Mode]

45. MIO2:

(DF12-40P Connector) Front Panel Connector

Function	Signal Name	Pin#		Signal Name	Function
Power LED+	PWR LED	2	1	HDD_LED-	HDD LED+
Power Button	Ground	4	3	USB0708_OC-	
	MIO_PSON	6	5	USB0910_OC-	
RESET	Ground	8	7	FP_RESET-	RESET
BUZZER	BUZZER-	10	9	BUZZER+	BUZZER
75111/GPIO23	GPIO_OUT1	12	11	GPIO_IN1	75111/GPIO27
75111/GPIO22	GPIO_OUT2	14	13	GPIO_IN2	75111/GPIO26
75111/GPIO21	GPIO_OUT3	16	15	GPIO_IN3	75111/GPIO25
75111/GPIO20	GPIO_OUT4	18	17	GPIO_IN4	75111/GPIO24
	5V_S5_USB	20	19	Ground	
PS/2 MOUSE	PS2_MSDATA	22	21	PS2_KBDATA	PS/2 Keyboard
	PS2_MSCLK	24	23	PS2_KBCLK	
USB2.0(USB10)	5V_S5_USB	26	25	5V_S5_USB	USB2.0(USB08)
	USB10_N	28	27	USB8_N	
	USB10_P	30	29	USB8_P	
	Ground	32	31	Ground	
USB2.0(USB11)	5V_S5_USB	34	33	5V_S5_USB	USB2.0(USB07)
	USB11_N	36	35	USB7_N	
	USB11_P	38	37	USB7_P	
	Ground	40	39	Ground	

Pin1-Ground: **HDD LED**. Use to connect hard disk activity LED. The LED blinks when the hard disk is reading or writing data.

Pin2-Ground: **Power LED**. Use to connect power LED. When the system is power on or under S0/S1 state, the LED is normally on; when the system is under S4/S5 state, the LED is off.

Pin4-6: **Power on/off Button**. Use to connect power switch button. The pins are disconnected under normal condition. You may short them temporarily to realize system startup& shutdown or awaken the system from sleep state.

Pin9-10: **Buzzer**. Use to connect an external buzzer.

Pin25-40: **USB7/USB8/USB10/USB11**. Front USB connectors with 4 USB2.0 ports via a dedicated USB cable.

Each USB Type A Receptacle (2 Ports) current value is limited under 2.0A. If the external USB device current exceeds 2.0A, please separate connectors into different Receptacle.

 Note:

When connecting LEDs, buzzer and USBs, please pay special attention to the signal polarity. Make sure that the connector pins have a one-to-one correspondence with the chassis wiring, or it may cause boot up failure.

46. PCIE_4x1 (option):

(4 x 20 Pin Connector) Riser Card expansion connector

It is able to support one PCIex4 or five PCIex1 signal. Both PCI express x1 and PCI express x4 support GEN1 and GEN2 mode.

Model	PCIe_4x1
TEG-M8172HT	Top
TEG-M8172HB	Bottom
TEG-M8172HB-S	Bottom

Riser Card	Function	TEG-M8172HB TEG-M8172HB-S	TEG-M8172HT
TX-F88P4	PCI slot x 4	●	X
Note: Please assemble the riser card correct, otherwise it will burn out the motherboard! If you do not know to assemble, please contact technical support.			

47. PCIE_16x1 (option):

(4x30 Pin) Riser Card expansion connector

It supports one PCIex16 or two PCIex8 signal with GEN1 and GEN2 mode.

Model	PCIE_16x1 connector
TEG-M8172HT	Top
TEG-M8172HB	Bottom
TEG-M8172HB-S	Bottom

Riser Card	Function	TEG-M8172HB TEG-M8172HB-S	TEG-M8172HT
TX-F88E41E16 R1.10	PCIe x4 slot x1 PCIe x16 slot x1	●	X
TX-F88E11E41E161	PCIe x1 slot x1 NA x1 PCIe x16 slot x1 PCIe x4 slot x1	●	X
TX-F88P1E161	PCIe x16 slot x1 PCI slot x1	●	X
TX-F88P2E41E161	PCIe x16 slot x1 PCIe x4 slot x1 PCI slot x1(NC) PCI slot x1	●	X
TX-F88E41E161E12P2	PCIe x4 slot x1 PCIe x16 slot x1 PCIe x1 slot x2 PCI slot x2	●	X
Note: Please assemble the riser card correct; otherwise it will burn out the motherboard! If you do not know how to assemble, please contact technical support.			

48. TPM_U1 (option):

Infineon's Trusted Platform Module (TPM2.0) SLB9665 is a fully standard compliant TPM based on the latest Trusted Computing Group (TCG) specification 2.0.

TPM_U1	SLB 9665 TT2.0
Model	TPM Function
TEG-M8172HT	X
TEG-M8172HB	●
TEG-M8172HB-S	X

49. I2C1 (option):

(2.0mm Pitch 1x4 wafer Pin Header) This function provides a set of I2C signals.

Pin#	Signal Name
1	3P3V_S0
2	Ground
3	MCU_I2C1_SDA
4	MCU_I2C1_SCL

Model	I2C1
TEG-M8172HB	X
TEG-M8172HB-S	●

50. DEBUG (option):

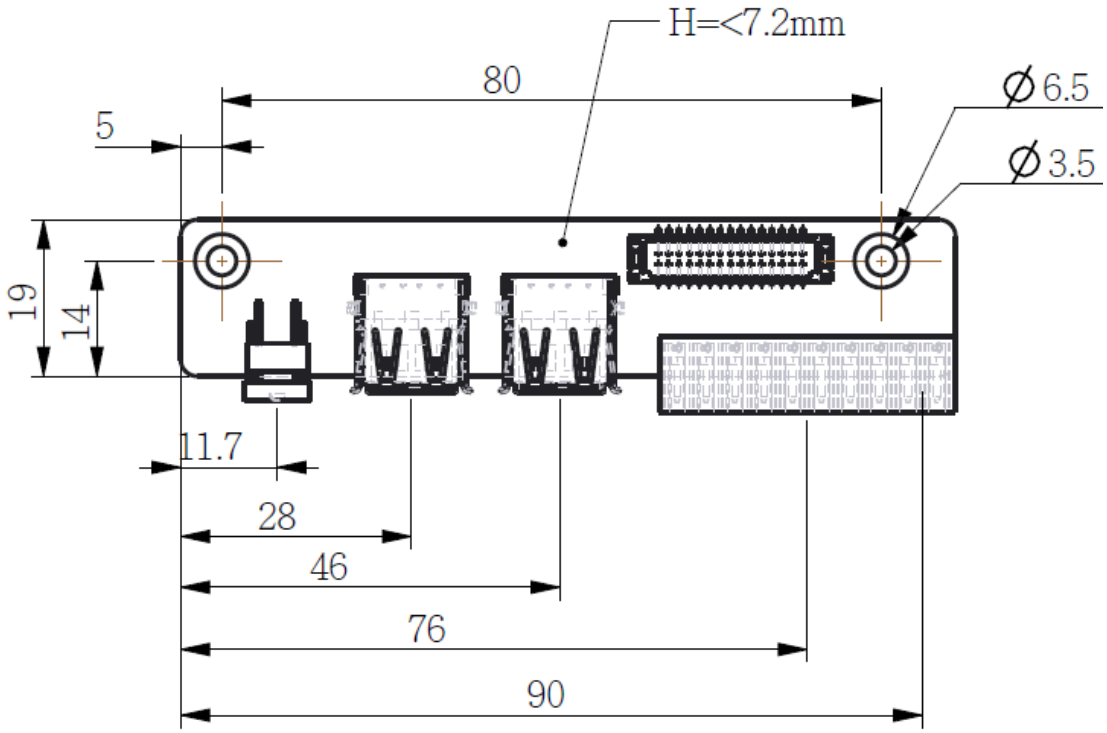
(2.0mm Pitch 1x9 Pin Header) Supports SPI signal

Pin#	Signal Name
1	LPC_FRAME-
2	LPC_AD3
3	LPC_AD2
4	LPC_AD1
5	LPC_AD0
6	Ground
7	PLT_RST_BUF1-
8	CLK_24M_DEBUG
9	3P3V_S0

51. JTAG1 (Reserve):

52. TX-F77 R1.00 (option):

TEG-M8172 I/O Card, connect to TEG-M8172 MIO2 with a dedicated cable.

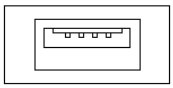


S1:

PWR BT: POWER on/off Button. Use to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state.

PWR LED: Indicates the status of POWER LED.

USB1:



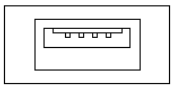
(Single stack USB type A, 2.0mm Pitch 1x4 box Pin Header) I/O USB connector

This connector provides one USB2.0 port with speed up to 480Mb/s.

Pin#	Signal Name
1	5V_USB78
2	USB7_N
3	USB7_P
4	Ground

USB1 and USB2 current value is limited under 1.5A.

If the external USB device current exceeds 1.5A, please separate connectors into different Receptacle.

USB2: 

(Single stack USB type A, 2.0mm Pitch 1x4 box Pin Header) I/O USB connector
This connector provides one USB2.0 port with speed up to 480Mb/s.

Pin#	Signal Name
1	5V_USB78
2	USB8_N
3	USB8_P
4	Ground

GPIO1:

(3.5mm Pitch 1x10 Pin Connector) General-purpose input/output port, provides a group of self-programming interfaces to customers for flexible use.

Pin#	Function
1	5V_GPIO (5V_S5_USB)
2	Ground
3	GPIO1 (GPIO_IN1)
4	GPIO2 (GPIO_IN2)
5	GPIO3 (GPIO_IN3)
6	GPIO4 (GPIO_IN4)
7	GPIO5 (GPIO_OUT1)
8	GPIO6 (GPIO_OUT2)
9	GPIO7 (GPIO_OUT3)
10	GPIO8 (GPIO_OUT4)

MIO1:

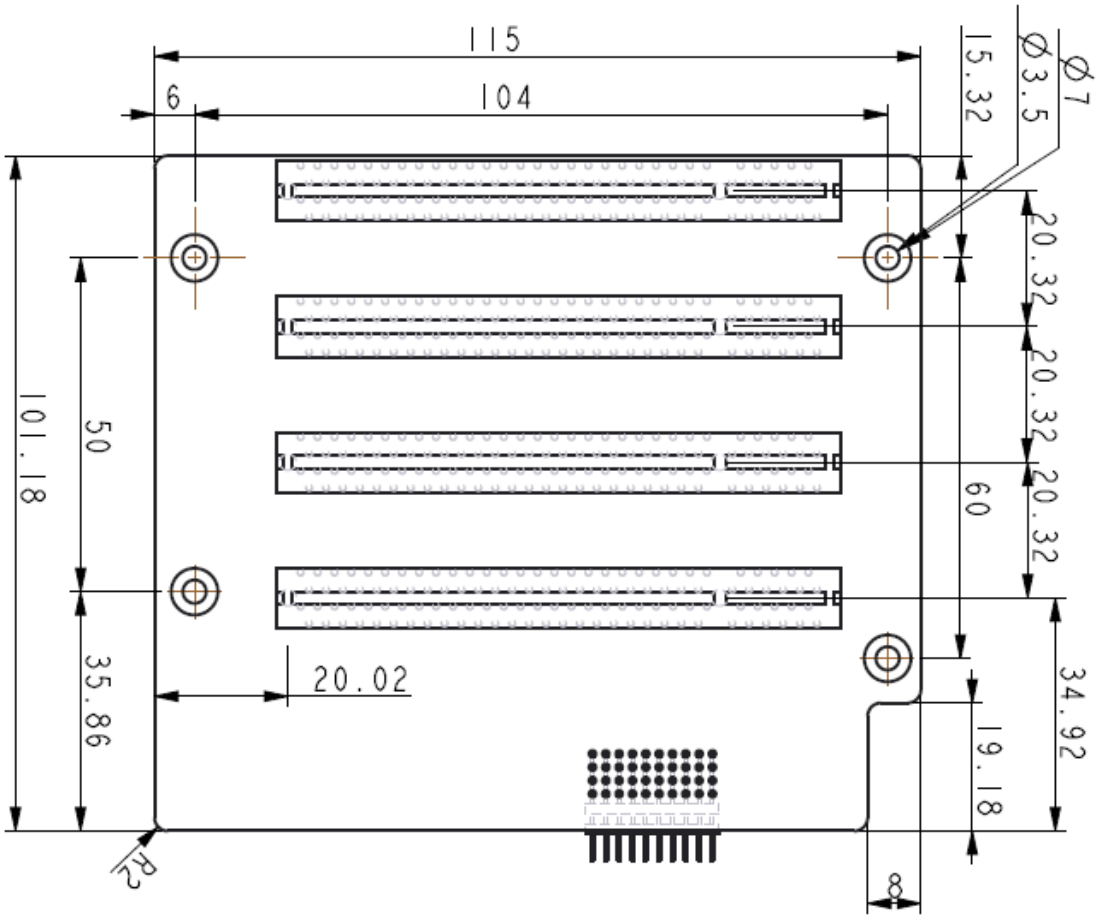
(DF 13-30P) TX-F77 MIO1 connects to TEG-M8172 MIO2 with a dedicated Y cable.

Signal Name	Pin#		Signal Name
PWR_LED	2	1	NC
Ground	4	3	USB0708_OC-
MIO_PSON-	6	5	NC
Ground	8	7	NC
NC	10	9	NC
GPIO_OUT1	12	11	GPIO_IN1
GPIO_OUT2	14	13	GPIO_IN2

GPIO_OUT3	16	15	GPIO_IN3
GPIO_OUT4	18	17	GPIO_IN4
NC	20	19	Ground
NC	22	21	NC
5V_S5_USB	24	23	5V_S5_USB
USB8_N	26	25	USB7_N
USB8_P	28	27	USB7_P
Ground	30	29	Ground

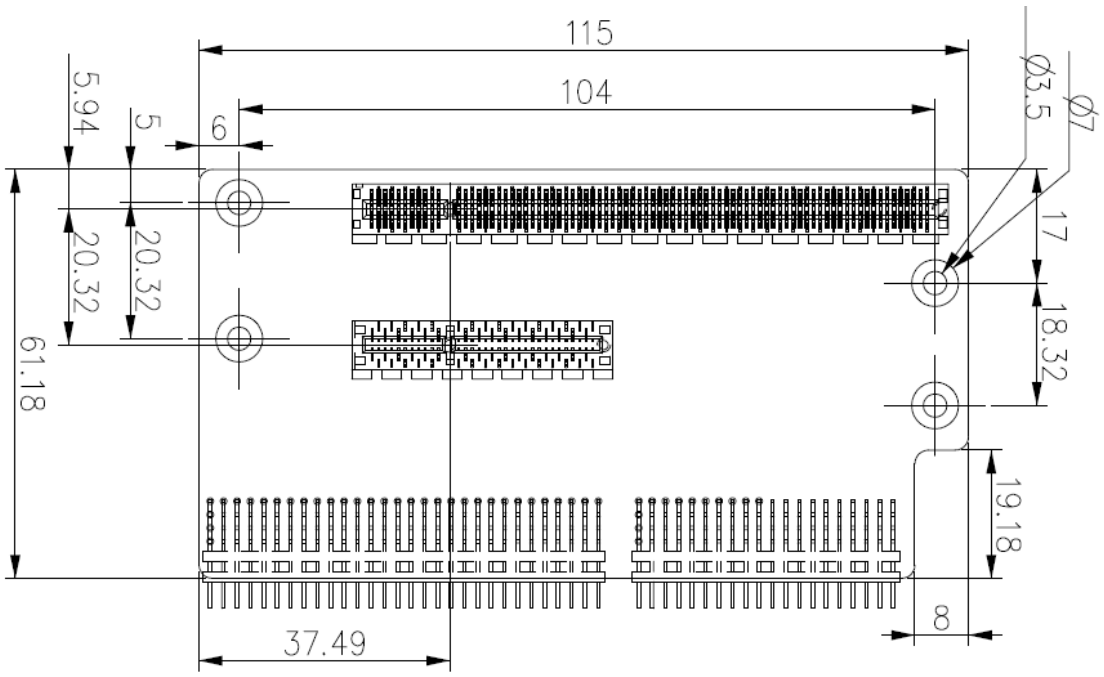
53. TX-F88P4 R1.00 (option):

TX-F88Ps connects to TEG-M8172HB PCIE_4x1 connector, PCIE_4x1, with four PCI slots, is located at the bottom.



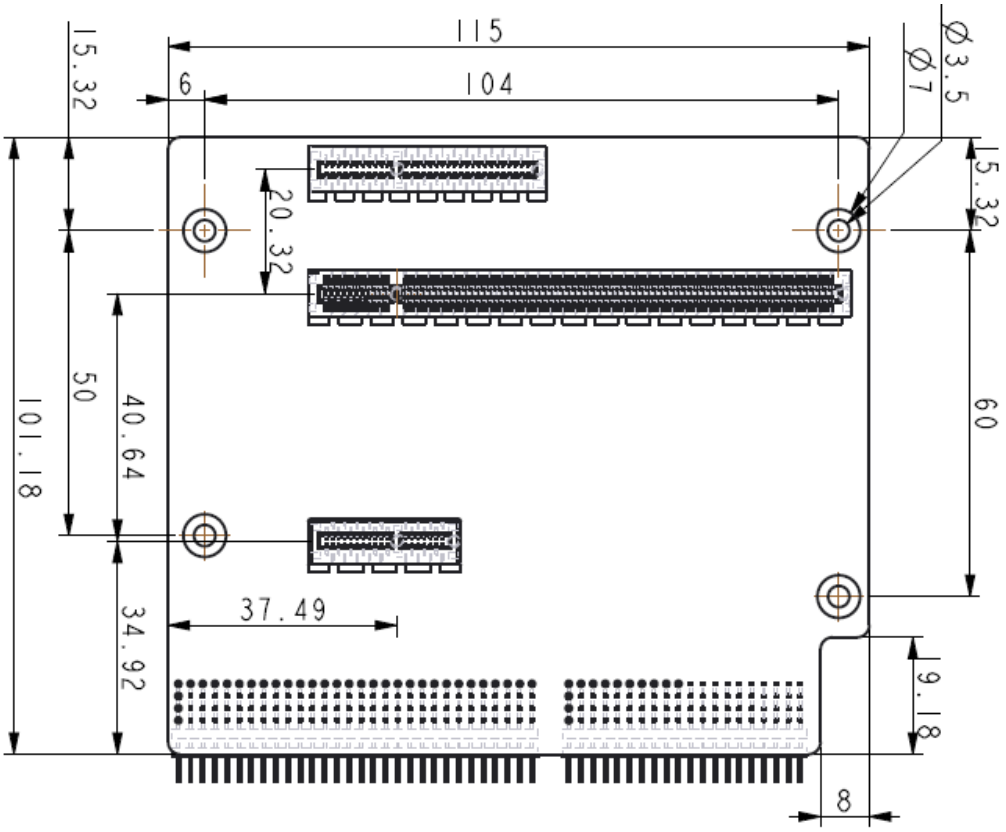
54. TX-F88E41E161 R1.10 (option):

TX-F88E41E161 connects to TEG-M8172HB PCIE_4x1 and PCIE_16x1 connector. PCIE_4x1 and 16x1, with4 and 16 PCI slots, located at the bottom.



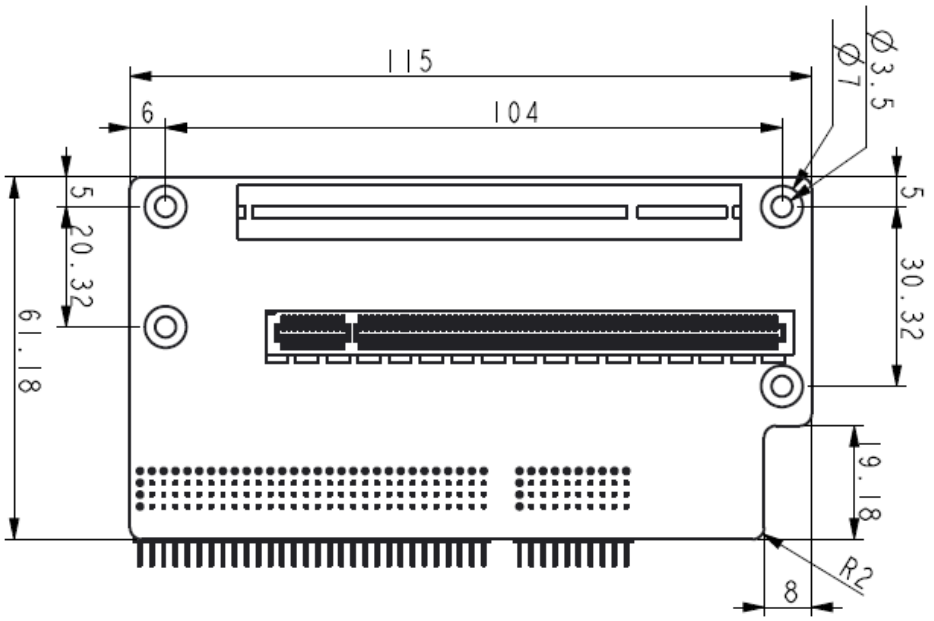
55. TX-F88E11E41E161 R1.00 (option):

TX-F88E11E41E161 connects to TEG-M8172HB PCIE_4x1 and PCIE_16x1 connector. PCIE_4x1 and 16x1, provide one PCIEx1 slot, one PCIEx4 slot and one PCIEx16 slot, are located at the bottom.



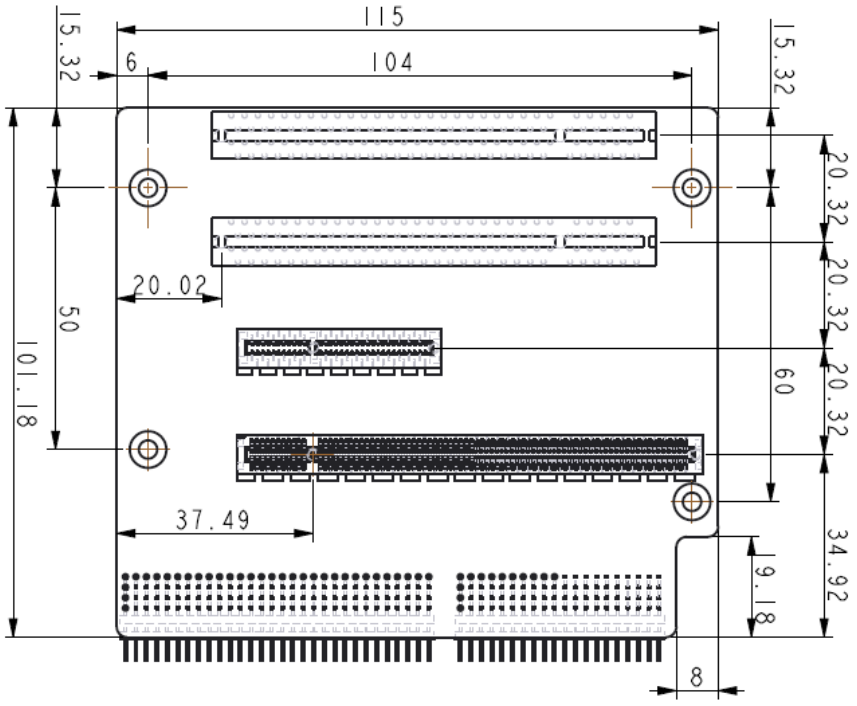
56. TX-F88P1E161 R1.00 (option):

TX-F88P1E161 connects to TEG-M8172HB PCIE_4x1 and PCIE_16x1 connector. PCIE_4x1 and PCIE_16x1, provide one PCI slot and one PCIEx16 slot, are located at the bottom.



57. TX-F88P2E41E161 R1.00 (option):

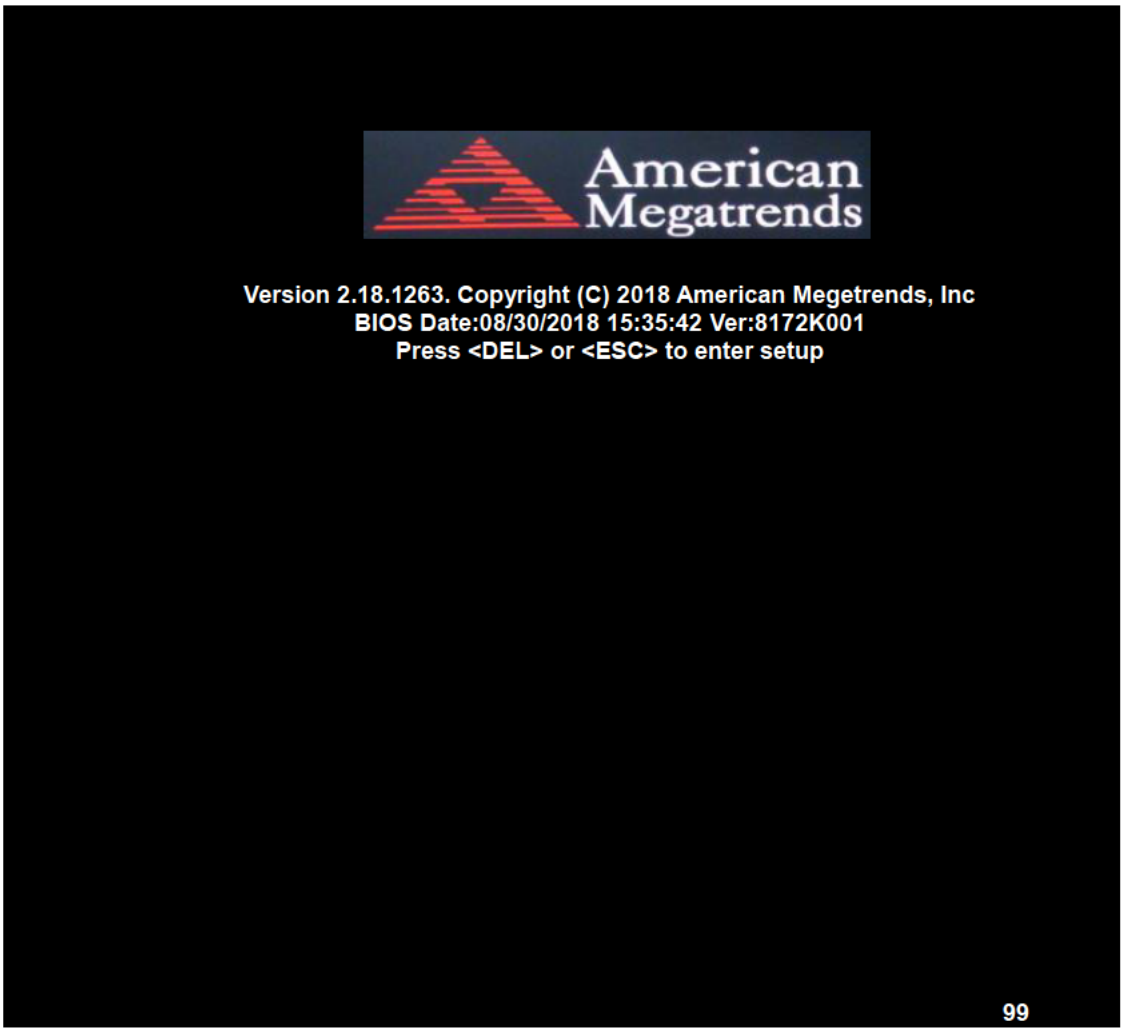
TX-F88P2E41E161 connects to TEG-M8172HB PCIE_4x1 and PCIE_16x1 connector. PCIE_4x1 and 16x1 provides two PCI slots, one PCIEx4 slot and one PCIEx16 slots, are located at the bottom.



Chapter 3 BIOS Setup

3.1 Operations after POST Screen

After CMOS discharge or BIOS flashing operation, press [Delete] key to enter CMOS Setup.

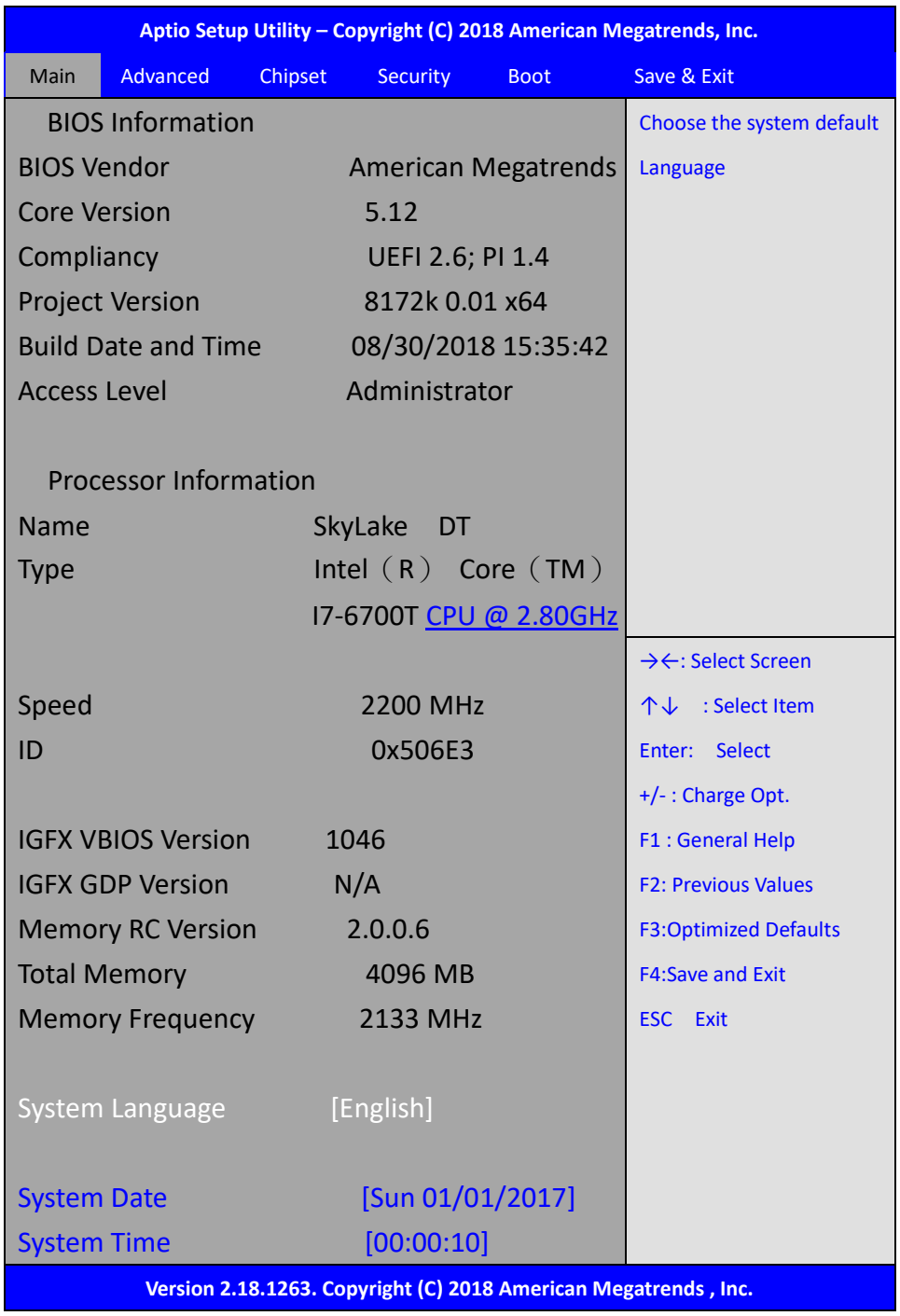


After optimizing, exits CMOS Setup.

3.2 BIOS Setup Utility

Press [Delete] key to enter BIOS Setup utility during POST, and then a main menu containing system summary information will appear.

3.3 Main Settings



System Time:

Set the system time, the time format is:

Hour :	0 to 23
Minute :	0 to 59
Second :	0 to 59

System Date:

Set the system date, the date format is:

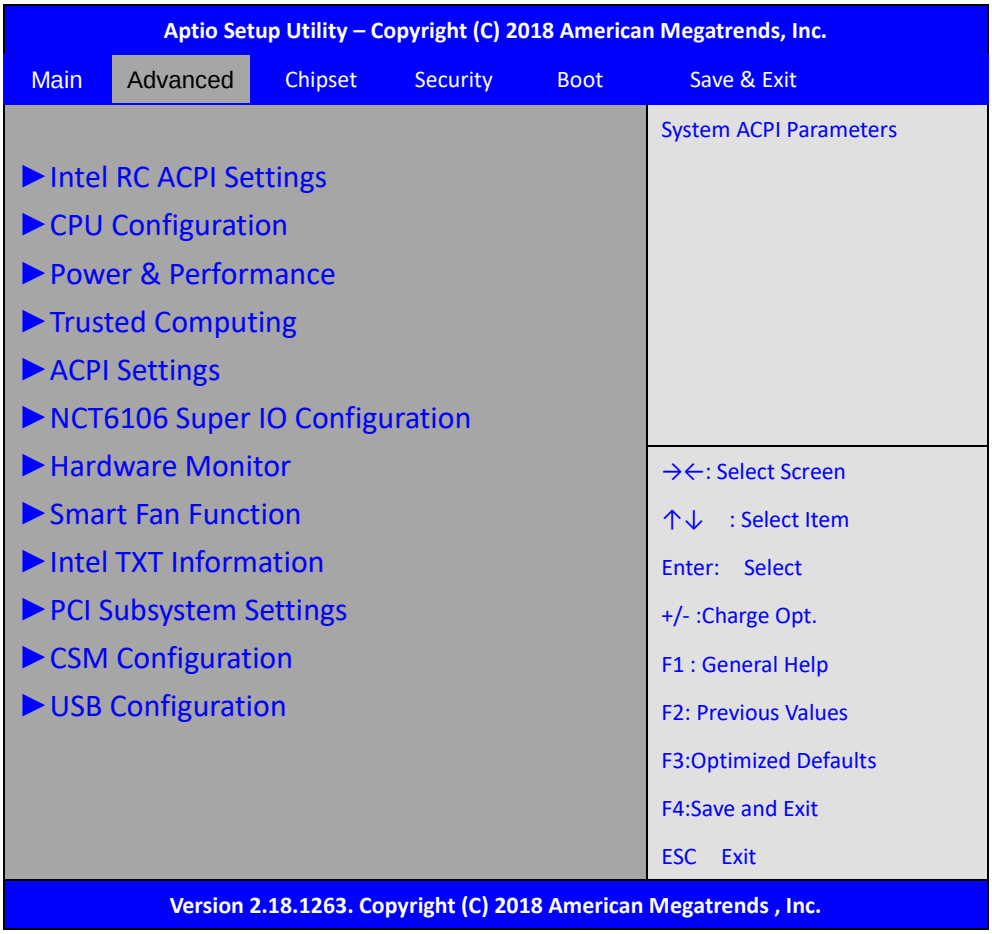
Day: Note that the 'Day' automatically changes when you set the date.

Month: 01 to 12

Date: 01 to 31

Year: 1998 to 2099

3.4 Advanced Settings



3.4.1 Intel RC ACPI Settings

PTID Support	**[Enabled]**
	[Disabled]
PECI Access Method	[**Direct I/O]**
	[ACPI
Native PCIE Enable	**[Enabled]**
	[Disabled]
Native ASPM	**[Auto]**
	[Enabled]
	[Disabled]

BDAT ACPI Table Support **[Disabled]**
[Enabled]

Wake system from S5 **[Disabled]**
[Enabled]
ACPI Debug **[Disabled]**
[Enabled]
Low Power S0 Idle Capability **[Disabled]**
[Enabled]
Lpit Recidency Counter **[SLP S0]**
[C10]

Interl Ready Mode Technology **[Disabled]**
[Enabled]

PCI Delay Optimization **[Disabled]**
[Enabled]
ZpODD Support **[Disabled]**
[Enabled]

3.4.2 CPU Configuration

Type	Intel（R）Core（TM）I3-6100 CPU@ 3.70GHz
ID	0x506E3
Speed	3700 MHz
L1 Date Cache	32 KB x 2
L1 Instruction Cache	32 KB x 2
L2 Cache	256 KB x 2
L3 Cache	3 MB
L4 Cache	

N/A	N/A
VMX	VMX
Supported	Supported
SMX/TXT	SMX/TXT
Not Supported	Not Supported
SW Guard Extensions(SGX) **[Software Controlled]**	SW Guard Extensions(SGX) **[Software Controlled]**
Select Owner EPOCH input type **[No Change In Owner EPOCHS]**	Select Owner EPOCH input type **[No Change In Owner EPOCHS]**

3.4.3 Power & Performance

►CPU – Power Management Control

Boot performance mode	**[Max Non-Turbo Performance]**
Intel(R) SpeedStep(tm)	**[Enabled]**
Race To Halt (RTH)	**[Enabled]**
Intel(R) Speed Shift Technology	**[Enabled]**
HDC Control	**[Enabled]**
Platform PL1 Enable	**[Disabled]**
Platform PL2 Enable	**[Disabled]**
Power Limit 4 Override	**[Disabled]**
C states	**[Enabled]**
Thermal Monitor	**[Enabled]**
Interrupt Redirection Mode Selection	**[PAIR with Fixed Priority]**
Timed MWAIT	**[Disabled]**
Energy Performance Gain	**[Disabled]**
EPG DIMM Idd3N	26
EPG DIMM Idd3P	11

► **View/Configure Turbo Options**

Configure Turbo Settings

Max Turbo Power Limit	4095.875
Min Turbo Power Limit	0.0

Package TDP Limit		35.0
Power Limit 1		35.0
Power Limit 2		43.750
1-core	Turbo	Ratio
27		
2-core	Turbo	Ratio
27		

Energy Efficient P-state	**[Enabled]**
Package Power Limit MSR Lock	**[Disabled]**
Power Limit 1 Override	**[Disabled]**
Power Limit 2 Override	**[Enabled]**
Power Limit 2	0
1-Core Ratio Limit Override	0
2-Core Ratio Limit Override	0
Energy Efficient Turbo	**[Enabled]**

►CPU VR Settings

PSYS Slope	0
PSYS Offset	0
PSYS Pmax Power	0

►Acoustic Noise Settings

Acoustic Noise Mitigation	**[Disabled]**

IA VR Domain	
Disable Fast PKG C Sate Ramp for IA Domain	[FALSE]
Slow Slew Rate for IA Domain	[FAST/2]

GT VR Domain	
Disable Fast PKG C Sate Ramp for IA Domain	[FALSE]
Slow Slew Rate for IA Domain	[FAST/2]

SA VR Domain	
Disable Fast PKG C Sate Ramp for IA Domain	[FALSE]

Slow Slew Rate for IA Domain	[FAST/2]
►Core/IA VR Settings	
VR Config Enable	**[Enabled]**
AC Loadline	0
DC Loadline	0
PS Current Threshold1	80
PS Current Threshold2	20
PS Current Threshold3	4
PS3 Enable	**[Enabled]**
PS4 Enable	**[Enabled]**
IMON Slope	0
IMON Offset	0
IMON Prefix	[+]
VR Current Limit	**0**
VR Voltage Limit	**0**
TDC Enable	**[Disabled]**
TDC Lock	**[Disabled]**
►GT-Sliced VR Settings	
VR Config Enable	**[Enabled]**
AC Loadline	0
DC Loadline	0
PS Current Threshold1	80
PS Current Threshold2	20
PS Current Threshold3	4
PS3 Enable	**[Enabled]**
PS4 Enable	**[Enabled]**
IMON Slope	0
IMON Offset	0
IMON Prefix	[+]
VR Config Limit	**0**
VR Voltage Limit	**0**
TDC Enable	**[Disabled]**
TDC Lock	**[Disabled]**
VR Mailbox Command options	0

►**Custom P-state Table**

Number of P states 0

►**Power Limit 3 Settings**

Power Limit 3 Override **[Disabled]**

►**CPU Lock Configuration**

CFG Lock **[Enabled]**

Overclocking Lock **[Disabled]**

►**GT – Power Management Control**

RC6(Render Standby) [Enabled]

Maximum GT frequency [Default Max Frequency]

3.4.4 Thermal Configuration

►**CPU Thermal Configuration**

DTS SMM **[Disabled]**

Tcc Activation Offset **0**

Tcc offset Time Window **[Disabled]**

Tcc offset Clamp Enable **[Disabled]**

Tcc offset Lock Enable **[Disabled]**

Bi-directional PROCHOT# **[Enabled]**

Disable PROCHOT# Output **[Enabled]**

Disable VR Thermal Alert# Output **[Disabled]**

PROCHOT Response **[Disabled]**

PROCHOT Lock **[Disabled]**

ACPI T-States **[Disabled]**

PECI Reset **[Disabled]**

PECI C10 Reset **[Disabled]**

►**Platform Thermal Configuration**

Automatic Thermal Reporting **[Disabled]**

Critical Trip Point **[119 C (POR)]**

Active Trip Point 0 **[71 C]**

Active Trip Point 0 Fan Speed **100**

Active Trip Point 1 **[55 C]**

Active Trip Point 1 Fan Speed **75**

Passive Trip Point **[95 C]**

Passive TC1 Value **1**

Passive TC2 Value **5**

Passive TSP Value **10**

Active Trip Points **[Enabled]**

Passive Trip Poinst **[Disabled]**

Critical Trip Points **[Enabled]**

PCH Thermal Device **[Enabled in PCI mode]**

PCH Temp Read **[Enabled]**

CPU Energy Read **[Enabled]**

CPU Temp Read **[Enabled]**

Alert Enable Lock **[Disabled]**

CPU Temp **72**

CPU Fan Speed **65**

►DPTF Configuration

3.4.5 Trusted Computing

TPM20 Device Found

Security Device Support **[Enabled]**

Active PCR banks SHA- 1, SHA256

Available PCR banks SHA- 1 , SHA256

Pending operation [None]

Platform Hierarchy [Enabled]

Storage Hierarchy [Enabled]

Endorsement Hierarchy [Enabled]

TPM2.0 UEFI Spec Version [TCG_ 2]

Physical Presence Spec a Version [1.3]

TPM 20 Interface Type [CRB]

Device Select [Auto]

3.4.6 ACPI Settings

Enable ACPI Auto Configuration:

[Disabled]

[Enabled]

Enable Hibernation: **[Enabled]**

[Disabled]

ACPI Sleep State: **[S3 (Suspend to RAM)]**

[Suspend Disabled]

Lock Legacy Resources:

[Disabled]
[Enabled]

S3 Video Repost:

[Disabled]
[Enabled]

3.4.7 NCT6106 Super IO Configuration

Super IO Chip NCT6106

►Serial Port 1 Configuration

Serial port **[Enabled]**
[Disabled]

Device Settings IO=3F8h IRQ=4；

Change Settings **[Auto]**

F75111 COM1 Config
[RS-232 Mode]
[RS-485 Mode]
[RS-422 Mode]

►Serial Port 2 Configuration

Serial port **[Enabled]**
[Disabled]

Device Settings IO=2F8h； IRQ=3；

Change Settings **[Auto]**

►Serial Port 3 Configuration

Serial port **[Enabled]**
[Disabled]

Device Settings IO=3E8h； IRQ=7；

Change Settings **[Auto]**

F75111 COM3 Config **[RS-485 Mode]**
[RS-422 Mode]

►Serial Port 4 Configuration

Serial port **[Enabled]**
[Disabled]

Device Settings IO=2E8h； IRQ=7；

Change Settings **[Auto]**

►Serial Port 5 Configuration

Serial port **[Enabled]**
[Disabled]
Device Settings IO=2F0h； IRQ=7；
Change Settings **[Auto]**

►Serial Port 6 Configuration

Serial port **[Enabled]**
[Disabled]
Device Settings IO=2E0h； IRQ=7；
Change Settings **[Auto]**

►Parallel Port Configuration

Parallel Port **[**Disabled**]**
Device Settings IO=378h； IRQ=5；

Change Settings **[Auto]**
Device Mode **[EPP-1.7 and SPP Mode]**
[STD Printer Mode]
[STD Mode]
[EPP-1.9 and SPP Mode]

3.4.8 Hardware Monitor

PC Health Status

CPU temperature ：+30 C
System temperature ：+36 C
SYS Fan Speed ：N/A
CPU Fan Speed ：1898 RPM
Vcore ：+1.024 V
12V ： ：+11.864 V
5V ： ：+5.160 V
1.5C ： ：+1.552 V

3.4.9 Smart FAN Function

PC Health Status

CPU Temperature1 35

CPU Temperature2	50
CPU Temperature3	65
CPU Temperature4	80
CPU Duty Cycle 1	100
CPU Duty Cycle 2	150
CPU Duty Cycle 3	200
CPU Duty Cycle 4	255
System Temperature 1	35
System Temperature 2	50
System Temperature 3	65
System Temperature 4	80
System Duty Cycle 1	100
System Duty Cycle 2	150
System Duty Cycle 3	190
System Duty Cycle 4	255

3.4.10 Intel TXT Information

Chipset	Production Fused
BiosAcm	Production Fused
Chipset Txt	Not Supported
Cput Txt	Not Supported
Error Code	None
Class Code	None
Major Code	None
Minor Code	None

3.4.11 PCI Subsystem Settings

AMI PCI Driver Version: A5.01.12

PCI Settings Common for all Devices:

Above 4G Decoding	**[Disabled]**
Hot-Piug Support	**[Enabled]**

Change Settings of the Following PCI Devices:

WARNING: Changing PCI Device(s) settings may have unwanted side effects!

System may HANG! PROCEED WITH CAUTION.

3.4.12 CSM Configuration

Compatibility Support Module Configuration

CSM Support	[Enabled]
CSM16 Module Version	07.81
GateA20 Active	**[Upon Request]**
Option ROM Messages	**[Force BIOS]**
INT19 Trap Response	**[Immediate]**
Boot option filter	**[UEFI and Legacy]**
Option ROM execution	
Network	**[Do not launch]**
Storage	**[UEFI]**
Video	**[Legacy]**
Other PCI devices	**[UEFI]**

3.4.13 USB Configuration

USB Module Version 19

USB Controllers:	1XHCI
USB Devices:	1 Keyboard, 1 Mouse
Legacy USB Support	**[Enabled]**
XHCI Hand-off	**[Enabled]**
USB Mass Storage Driver Support	**[Enabled]**
Port 60/64 Emulation	**[Disabled]**
USB Hardware delays and time-outs:	
USB transfer time-out	**[20 sec]**
Device reset time-out	**[20 sec]**
Device power-up delay	**[Auto]**

3.5 Chipset Settings

3.5.1 System Agent (SA) Configuration

SA PCIe Code Version	1.9.0.0
VT-d	Supported
Stop Grant Configuration	**[Auto]**
VT-d	**[Enabled]**
►Memory Configuration	
Memory RC Version	2.0.0.6
Memory Frequency	2133MHz
Memory Timings (Tcl-Trcd-TRP-TRAS)	15-15-15-36
Channel 0 Slot 0	Not Populated / Disabled
Channel 0 Slot 1	Not Populated / Disabled
Channel 1 Slot 0	Populated/&Enabled
Size	8192 MB (DDR4)

Number of Ranks	2
Manufacturer	Transcend
Channel 1 Slot 1	Not Present / Disabled

Memory ratio/reference clock Options moved to Overclock->Menmory->Custom Profile menu	
MRC ULT Safe Conifg	**[Disabled]**
Maximum Memory Frequency	**[Auto]**
HOB Buffer Size	**[Auto]**
ECC Support	**[Enabled]**
Max TOLUD	**[Dynamic]**
SA GV	**[Enabled]**
SA GV Low Freq	**[MRC default]**
Retrain on Fast fail	**[Enabled]**
Command Tristate	**[Enabled]**
Enable RH Prevention	**[Enabled]**
Row Hammer Solution	**[Hardware RHP]**
RH Activation Probability	**[1/2^11]**
Exit On Failure(MRC)	**[Enabled]**
MC Lock	**[Enabled]**
Probeless Trace	**[Disabled]**
Enable/Disable IED(Intel Enhanced Debug)	**[Disabled]**
Ch Hash Support	**[Enabled]**
Ch Hash Mask	**12488**
Ch Hash Interleaved Bit	**[BIT8]**
VC1 Read Metering	**[Enabled]**
VC1 RdMeter Time Window	**800**
VC1 RdMeter Threshold	**280**
Strong Weak Leaker	**7**
Memory Scrambler	**[Enabled]**
Force ColdReset	**[Disabled]**
Channel A DIMM Control	**[Enable both DIMMS]**
Channel B DIMM Control	**[Enable both DIMMS]**
Force Single Rank	**[Disabled]**
Memory Remap	**[Enabled]**
Time Measure	**[Disabled]**

DLL Weak Lock Support **[Enabled]**

Pwr Down Idle Timer 0

Mrc Fast Boot **[Enabled]**

Lpddr Mem WL Set **[Set B]**

EV Loader **[Disabled]**

EV Loader Delay **[Enabled]**

►Memory Thermal Configuration

►Memory Power and Thermal Throttling

DDR PowerDown and idle counter **[BIOS]**

For LPDDR Only:DDR PowerDown and idle counter **[BIOS]**

REFRESH_2X_MODE **[Disabled]**

LPDDR Thermal Sensor **[Enabled]**

SelfRefresh Enable **[Enabled]**

SelfRefresh IdleTimer 512

Throttler CKEMin Defeature **[Disabled]**

Throttler CKEMin Timer 48

►Dram Power Meter

Use user provided power weights, scale factor, and channel power floor values **[Disabled]**

Energy Scale factor 4

Idle Energy Ch0Dimm0 10

PowerDown Energy Ch0Dimm0 6

Activate Energy Ch0Dimm0 172

Read Energy Ch0Dimm0 212

Write Energy Ch0Dimm0 221

Idle Energy Ch0Dimm1 10

PowerDown Energy Ch0Dimm1 6

Activate Energy Ch0Dimm1 172

Read Energy Ch0Dimm1 212

Write Energy Ch0Dimm1 221

Idle Energy Ch1Dimm0	10
PowerDown Energy Ch1Dimm0	6
Activate Energy Ch1Dimm0	172
Read Energy Ch1Dimm0	212
Write Energy Ch1Dimm0	221
Idle Energy Ch1Dimm1	10
PowerDown Energy Ch1Dimm1	6
Activate Energy Ch1Dimm1	172
Read Energy Ch1Dimm1	212
Write Energy Ch1Dimm1	221

►**Memory Thermal Reporting**

Lock Thermal:Management Registers	**[Enabled]**

Memory Thermal Reporting

Extern Therm Status	**[Disabled]**
Closed Loop Therm Manage	**[Disabled]**
Open Loop Therm Manage	**[Disabled]**

Thermal Threshold Settings

Warm Threshold Ch0 Dimm0	255
Warm Threshold Ch0 Dimm1	255
Hot Threshold Ch0 Dimm0	255
Hot Threshold Ch0 Dimm1	255
Warm Threshold Ch1 Dimm0	255
Warm Threshold Ch1 Dimm1	255
Hot Threshold Ch1 Dimm0	255
Hot Threshold Ch1 Dimm1	255

Thermal Throttle Budget Settings

Warm Budget Ch0 Dimm0	255
Warm Budget Ch0 Dimm1	255
Hot Budget Ch0 Dimm0	255
Hot Budget Ch0 Dimm1	255
Warm Budget Ch1 Dimm0	255

Warm Budget Ch1 Dimm1	255
Hot Budget Ch1 Dimm0	255
Hot Budget Ch1 Dimm1	255

►Memory RAPL

Rapl Power Floor Ch0	0
Rapl Power Floor Ch1	0

RAPL PL Lock	**[Disabled]**
RAPL PL 1 enable	**[Disabled]**
RAPL PL 1 Power	0
RAPL PL 1 WindowX	0
RAPL PL 1 WindowY	0

RAPL PL 2 enable	**[Disabled]**
RAPL PL 2 Power	222
RAPL PL 2 WindowX	1
RAPL PL 2 WindowY	10

Memory Thermal Management **[Disabled]**

►Memory Training Algorithms

Early Command Training	**[Disabled]**
SenseAmp Offset Training	**[Enabled]**
Early ReadMPR Timing Centering 2D	**[Enabled]**
Read MPR Training	**[Enabled]**
Receive Enable Training	**[Enabled**]
Jedec Write Leveling	**[Enabled]**
Early Write Time Centering 2D	**[Enabled]**
Early Write Drive Strength/Equalization	**[Enabled]**
Early Read Time Centering 2D	**[Enabled]**
Write Timing Centering 1D	**[Enabled]**
Write Voltage Centering 1D	**[Enabled]**
Read Timing Centering 1D	**[Enabled]**
Dimm ODT Training*	**[Enabled]**
Max RTT_WR	**[ODT Off]**
DIMM RON Training*	**[Enabled]**

	Write Drive Strength/Equalization	**[Disabled]**
2D*		
	Write Slew Rate Training*	**[Enabled]**
	Read ODT Training*	**[Enabled]**
	Read Equalization Training*	**[Enabled]**
	Read Amplifier Training*	**[Enabled]**
	Write Timing Centering 2D	**[Enabled]**
	Read Timing Centering 2D	**[Enabled]**
	Command Voltage Centering	**[Enabled]**
	Write Voltage Centering 2D	**[Enabled]**
	Read Voltage Centering 2D	**[Enabled]**
	Late Command Training	**[Enabled]**
	Round Trip Latency	**[Enabled]**
	Turn Around Timing Training	**[Enabled]**
	Rank Margin Tool	**[Disabled]**
	Memory Test	**[Disabled]**
	DIMM SPD Alias Test	**[Enabled]**
	Receive Enable Centering 1D	**[Enabled]**
	Retrain Margin Check	**[Enabled]**
	Write Drive Strength Up/Dn Independently	**[Disabled]**
	CMD Slew Rate Traning	**[Enabled]**
	CMD Drive Strength / Tx Equalization	**[Enabled]**
	CMD Normalization	**[Enabled]**
	►Graphics Configuration	
	Graphics Turbo IMON Current	31
	Skip Scanning of External Gfx Card	**[Disabled]**
	Primary Display	**[Auto]**
	Select PCIE Card	**[Auto]**
	Internal Graphics	**[Auto]**
	GTT Size	**[8MB]**
	Aperture Size	**[256MB]**
	DVMT Pre-Allocated	**[32M]**
	DVMT Total GFx Mem	**[256M]**
	GFx Low Power Mode	**[Enabled]**

VDD Enable	**[Enabled]**
HDCP Support	[**Enabled]**
Algorithm	[**One-time]**
PM Support	**[Enabled]**
PAVP Enable	**[Enabled]**
Cdynmax Clamping Enable	**[Enabled]**
Cd Clock Frequency	**[675Mhz]**
IUER Button Enable	**[Disabled]**

►External GFx Primary Dispiay Configuration

Primary PEG	**[Auto]**
Primary PCIE	**[Auto]**

►LCD Control

Primary IGFX Boot Dispaly	**[HDMI]**
Secondary IGFX Boot Dispaly	**[VGA]**
LCD Panel Type	**[VBIOS Default]**
Panel Scanling	**[Auto]**
Backlight Control	**[PWM Normal]**
Active LFP	**[eDP Port-A]**
Panel Color Depth	**[18 Bit]**
Backlight Brightness	**255**

►DMI/OPI Configuration

DMI	X4 Gen3
DMI Max Link Speed	**[Auto]**
DMI Gen3 Eq Phase 2	**[Auto]**
DMI Gen3 Eq Phase 3 Method	**[Auto]**
DMI Vc1 Control	**[Disabled]**
DMI Vcm Control	**[Enabled]**
Program Static Phase1 Eq	**[Enabled]**
DMI Link ASPM Control	**[L1]**
DMI Extended Sync Control	**[Disabled]**
DMI De-emphasis Control	**[-3.5 dB]**
DMI IOT	**[Disabled]**

► **Gen3 Root Port Preset value for each Lane**

Lane 0	**4**
Lane 1	**4**
Lane 2	**4**
Lane 3	**4**

► **Gen3 Endpoint Preset value for each Lane**

Lane 0	**7**
Lane 1	**7**
Lane 2	**7**
Lane 3	**7**

► **Gen3 Endpoint Hint value for each Lane**

Lane 0	**2**
Lane 1	**2**
Lane 2	**2**
Lane 3	**2**

► **Gen3 RxCTLE Control**

Bundle0	**3**
Bundle1	**3**

►**PEG Port Configuration**

PEG 0:1:0	x4 Gen2
Enable Root Port	**[Auto]**
Max Link Speed	**[Auto]**
Max Link Width	**[Auto]**
Power Down Unused Lanes	**[Auto]**
Gen3 Eq Phase 2	**[Auto]**
Gen3 Eq Phase 3 Method	**[Auto]**
ASPM	**[Auto]**
De-emphasis Control	**[-3.5 dB]**
OBFF	**[Enabled]**
LTR	**[Enabled]**
PEG0 Slot Power Limit Value	**75**
PEG0 Slot Power Limit Scale	**[1.0x]**
PEG0 Slot Power Limit Number	**1**
PEG 0:1:1	Not Present
Enable Root Port	**[Auto]**

Max Link Speed	**[Auto]**
PEG1 Slot Power Limit Value	**75**
PEG1 Slot Power Limit Scale	**[1.0x]**
PEG1 Slot Power Limit Number	**2**
PEG 0:1:2	Not Present
Enable Root Port	**[Auto]**
Max Link Speed	**[Auto]**
PEG2 Slot Power Limit Value	**75**
PEG2 Slot Power Limit Scale	**[1.0x]**
PEG2 Slot Power Limit Number	**3**

Program PCIe ASPM after opROM	**[Disabled]**
Program Static Phase1 Eq	**[Enabled]**

Gen3 Adaptive Software Equalization	
Always Attempt SW EQ	**[Disabled]**
Nimber of Presets to test	**[Auto]**
Allow PERST# GPIO Usage	**[Enabled]**
SW EQ Enable VOC	**[Auto]**
Jitter Dwell Time	**3000**
Jitter Error Target	**2**
VOC Dwell Time	**10000**
VOC Error Target	**2**
Generate BDAT PEG Margin Date	**[Disabled]**
PCIe Rx CEM Test Mode	**[Disabled]**
PCIe Spread Spectrum Clocking	**[Enabled]**

►PEG Port Feature Configuration

Detect Non-Compliance Device	**[Disabled]**

►Gen3 Root Port Preset value for each Lane

Lane 0	**7**
Lane 1	**7**
Lane 2	**7**
Lane 3	**7**
Lane 5	**7**
Lane 6	**7**

Lane 7	**7**
Lane 8	**7**
Lane 9	**7**
Lane 10	**7**
Lane 11	**7**
Lane 12	**7**
Lane 13	**7**
Lane 14	**7**
Lane 15	**7**

► **Gen3 Endpoint Preset value for each Lane**

Lane 0	**7**
Lane 1	**7**
Lane 2	**7**
Lane 3	**7**
Lane 5	**7**
Lane 6	**7**
Lane 7	**7**
Lane 8	**7**
Lane 9	**7**
Lane 10	**7**
Lane 11	**7**
Lane 12	**7**
Lane 13	**7**
Lane 14	**7**
Lane 15	**7**

► **Gen3 Endpoint Hint value for each Lane**

Lane 0	**2**
Lane 1	**2**
Lane 2	**2**
Lane 3	**2**
Lane 5	**2**
Lane 6	**2**
Lane 7	**2**
Lane 8	**2**
Lane 9	**2**
Lane 10	2
Lane 11	**2**

Lane 12	**2**
Lane 13	**2**
Lane 14	**2**
Lane 15	**2**

► **Gen3 RxCTLE Control**

Bundle0	**0**
Bundle2	**0**
Bundle3	**0**
Bundle4	**0**
Bundle5	**0**
Bundle6	**0**
Bundle7	**0**
RxCTLE Override	**[Disabled]**

6.5.2 PCH-IO Configuration

DCI enable (HDCIEN)	[Disabled]
Debug Port Selection	[Legacy UART]
Serial IRQ Mode	[Continuous]
State After G3	[S5 State]
F75111 GPIO20 Config	[Output]
F75111 GPIO20 Output Setting	[Low]
F75111 GPIO21 Config	[Output]
F75111 GPIO21 Output Setting	[Low]
F75111 GPIO22 Config	[Output]
F75111 GPIO22 Output Setting	[Low]
F75111 GPIO23 Config	[Output]
F75111 GPIO23 Output Setting	[Low]
F75111 GPIO24 Config	[Output]
F75111 GPIO24 Output Setting	[Low]
F75111 GPIO25 Config	[Output]
F75111 GPIO25 Output Setting	[Low]
F75111 GPIO26 Config	[Output]
F75111 GPIO26 Output Setting	[Low]
F75111 GPIO27 Config	[Output]
F75111 GPIO27 Output Setting	[Low]
F75111 COM1 Config	[RS232 mode]
F75111 COM2 Config	[RS232 mode]

F75111 COM3 Config [RS485 mode]
F75111 COM6 Config [RS232 mode]
Port 80h Redirecton [LPC Bus]

►PCI Express Configuration
PCI Express Clock Gating [Enabled]
Legacy IO Low Latency [Disabled]
DMI Link ASPM Control [Enabled]
PCIE Port assigned to LAN Disabled
Port8xh Decode [Disabled]
Peer Memory Write Enable [Disabled]
Compliance Test Mode [Disabled]
PCIe-USB Glitch W/A [Disabled]
PCIe function swap [Enabled]

►PCI Express Gen3 Eq Lanes
PCIE1 Cm 6
PCIE1 Cp 2
PCIE2 Cm 6
PCIE2 Cp 2
PCIE3 Cm 6
PCIE3 Cp 2
PCIE4 Cm 6
PCIE4 Cp 2
PCIE5 Cm 6
PCIE5 Cp 2
PCIE6 Cm 6
PCIE6 Cp 2
PCIE7 Cm 6
PCIE7 Cp 2
PCIE8 Cm 6
PCIE8 Cp 2
PCIE9 Cm 6
PCIE9 Cp 2
PCIE10 Cm 6
PCIE10 Cp 2
PCIE11 Cm 6
PCIE11 Cp 2

PCIE12 Cm	6
PCIE12 Cp	2
PCIE13 Cm	6
PCIE13 Cp	2
PCIE14 Cm	6
PCIE14 Cp	2
PCIE15 Cm	6
PCIE15 Cp	2
PCIE16 Cm	6
PCIE16 Cp	2
PCIE17 Cm	6
PCIE17 Cp	2
PCIE18 Cm	6
PCIE18 Cp	2
PCIE19 Cm	6
PCIE19 Cp	2
PCIE20 Cm	6
PCIE20 Cp	2

Override SW EQ Settings	[Disabled]

►PCI Express Root Port 1

PCI Express Root Port 1	[Enabled]
Topology	[Unknown]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]

PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE1 LTR [Enabled]
Snoop Latency Override [Auto]
Non Snoop Latency Override [Auto]
Force LTP Override [Disabled]

PCIE1 LTR Lock [Disabled]

PCH PCIe CLKRRQ# Configuration
PCIE CLKRRQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 2
PCI Express Root Port 2 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]

NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
PCH PCIE2 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE2 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE2 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 3
PCI Express Root Port 3 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]

UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
PCH PCIE3 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE3 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE3 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 4
PCI Express Root Port 4 [Enabled]
Topology [Unknown]

ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE4 LTR [Enabled]

Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE4 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE4 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]

Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 5
PCI Express Root Port 5 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE5 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE5 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration

PCIE5 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]

Prefetchable Memory 10

Reseved Memory Alignment 1

Prefetchable Memory Alignment 1

►PCI Express Root Port 6

PCI Express Root Port 6 [Enabled]

Topology [Unknown]

ASPM [Auto]

L1 SubStates [L1.1&L1.2]

Gen3 Eq Phase3 Method [Software Search]

UPTP 5

DPTP 7

ACS [Enabled]

URR [Disabled]

FER [Disabled]

NFER [Disabled]

CER [Disabled]

CTO [Disabled]

SEFE [Disabled]

SENFE [Disabled]

SECE [Disabled]

PME SCI [Enabled]

Hot Plug [Disabled]

Advanced Error Reporting [Enabled]

PCIe Speed [Gen2]

Transmitter Half Swing [Disabled]

Detect Timeout 0

Extra Bus Reserved 0

Reserved Memory 10

Reserved I/O 4

PCH PCIe LTR Configuration

PCH PCIE6 LTR [Enabled]

Snoop Latency Override [Auto]

Non-Snoop Latency Override [Auto]

Force LTR Override [Disabled]

PCIE6 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE6 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 7
PCI Express Root Port 7 [Enabled]
Topology [X1]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Gen2]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 7
Reserved Memory 17
Reserved I/O 16
PCH PCIe LTR Configuration
PCH PCIE7 LTR [Enabled]

Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE7 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE7 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 8
PCI Express Root Port 8 [Enabled]
Topology [X1]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 7
Reserved Memory 17

Reserved I/O 8

PCH PCIe LTR Configuration
PCH PCIE8 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE8 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE8 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reserved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 9
PCI Express Root Port 9 [Enabled]
Topology [X4]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]

Transmitter Half Swing [Disabled]

Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE9 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE9 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE9 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 13
PCI Express Root Port 13 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]

SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]

Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
PCH PCIE13 LTR [Enabled]
Snoop Latency Override [Auto]
Non Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE13 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE13 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 14
PCI Express Root Port 14 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]

FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]

Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE14 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE14 LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE14 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 15
PCI Express Root Port 15 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]

Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4
PCH PCIe LTR Configuration	
PCH PCIE15 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]
PCIE15 LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE15 CLKREQ Mapping Override	[Default]
►Extra options	
Detect Non-Compliance Device	[Disabled]
Prefetchable Memory	10
Reseved Memory Alignment	1
Prefetchable Memory Alignment	1

►PCI Express Root Port 16

PCI Express Root Port 16	[Enabled]
Topology	[Unknown]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4

PCH PCIe LTR Configuration

PCH PCIE16 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]

PCIE16 LTR Lock	[Disabled]

PCH PCIe CLKREQ# Configuration

PCIE16 CLKREQ Mapping Override	[Default]

►Extra options

Detect Non-Compliance Device	[Disabled]
Prefetchable Memory	10
Reseved Memory Alignment	1
Prefetchable Memory Alignment	1

►PCI Express Root Port 17

PCI Express Root Port 17	[Enabled]
Topology	[M2]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4

PCH PCIe LTR Configuration

PCH PCIE17 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]

Force LTR Override [Disabled]

PCIE17 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE17 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 19
PCI Express Root Port 19 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10

Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE19 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE19LTR Lock [Disabled]
PCH PCIe CLKREQ# Configuration
PCIE19 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 21
PCI Express Root Port 21 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]

PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE21 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE21 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE21 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 22
PCI Express Root Port 22 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]

SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
PCH PCIE22 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE22 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE22 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 23
PCI Express Root Port 23 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]

URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4
PCH PCIe LTR Configuration
PCH PCIE23 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]
PCIE23 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE23 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 24
PCI Express Root Port 24 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]

Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4

PCH PCIe LTR Configuration

PCH PCIE24 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]

PCIE24 LTR Lock	[Disabled]

PCH PCIe CLKREQ# Configuration

PCIE24 CLKREQ Mapping Override	[Default]

►Extra options

Detect Non-Compliance Device	[Disabled]
Prefetchable Memory	10
Reseved Memory Alignment	1
Prefetchable Memory Alignment	1

►SATA And RST Configuration

SATA Controller(s)	[Enabled]
SATA Mode Selection	[AHCI]
SATA Test Mode	[Disabled]
Aggressive LPM Support	[Enabled]
SATA Controller Speed	[Default]
Serial ATA Port 0	Empty
Software Preserve	Unknown
Port 0	[Enabled]
Hot Plug	[Disabled]
Configured as ESATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[ISATA]
SATA Port 0 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 1	Empty
Software Preserve	Unknown
Port 1	[Enabled]
Hot Plug	[Disabled]
Configured as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[ISATA]
SATA Port 1 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 2	Empty
Software Preserve	Unknown
Port 2	[Enabled]
Hot Plug	[Disabled]
Configured as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]

Topology	[ISATA]
SATA Port 2 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 3	Empty
Software Preserve	Unknown
Port 3	[Enabled]
Hot Plug	[Disabled]
Configured as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[ISATA]
SATA Port 3 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 4	Empty
Software Preserve	Unknown
Port 4	[Enabled]
Hot Plug	[Disabled]
Configurded as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 4 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 5	WDC WD5000LPVX (500.1GB)
Software Preserve	SUPPORTED
Port 5	[Enabled]
Hot Plug	[Disabled]
Configurded as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 5 DevSlp	[Disabled]

DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 6	Empty
Software Preserve	Unknown
Port 6	[Enabled]
Hot Plug	[Disabled]
Configurded as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 6 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 7	Empty
Software Preserve	Unknown
Port 7	[Enabled]
Hot Plug	[Disabled]
Configured as eSATA	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 7 DevSlp	[Disabled]
DIT0 Configuration	[Disabled]
DIT0 Value	625
DM Value	15

►Software Feature Mask Configuration

HDD Unlock	[Enabled]
LED Locate	[Enabled]

►USB Configuration

XHCI Disable Compliance	[FALSE]
XDCI Support	[Disabled]
USB Port Disable Override	[Disabled]

3.6 Security Settings

3.6.1 Administrator Password

3.6.2 User Password

Type the password with up to 20 characters and then press <Enter> key. This will clear all previously typed CMOS passwords. You will be requested to confirm the password. Type the password again and press <Enter> key. You may press <Esc> key to abandon password entry operation.

To clear the password, just press <Enter> key when password input window pops up. A confirmation message will be shown on the screen as to whether the password will be disabled.

You will have direct access to BIOS setup without typing any password after system reboot once the password is disabled.

Once the password feature is used, you will be requested to type the password each time you enter BIOS setup. This will prevent unauthorized persons from changing your system configurations.

Also, the feature is capable of requesting users to enter the password prior to system boot to control unauthorized access to your computer. Users may enable the feature in Security Option of Advanced BIOS Features. If Security Option is set to System, you will be requested to enter the password before system boot and when entering BIOS setup; if Security Option is set to Setup, you will be requested for password for entering BIOS setup.

3.6.3 Secure Boot

System Mode	Setup
Secure Boot	Not Active
Vendor Keys	Active
Attempt Secure Boot	**[Disabled]**
Secure Boot Mode	**[Custom]**

►Key Management

Provision Factory Defaults	**[Disabled]**

►Install Factory Default keys

►Enroll Efi Image

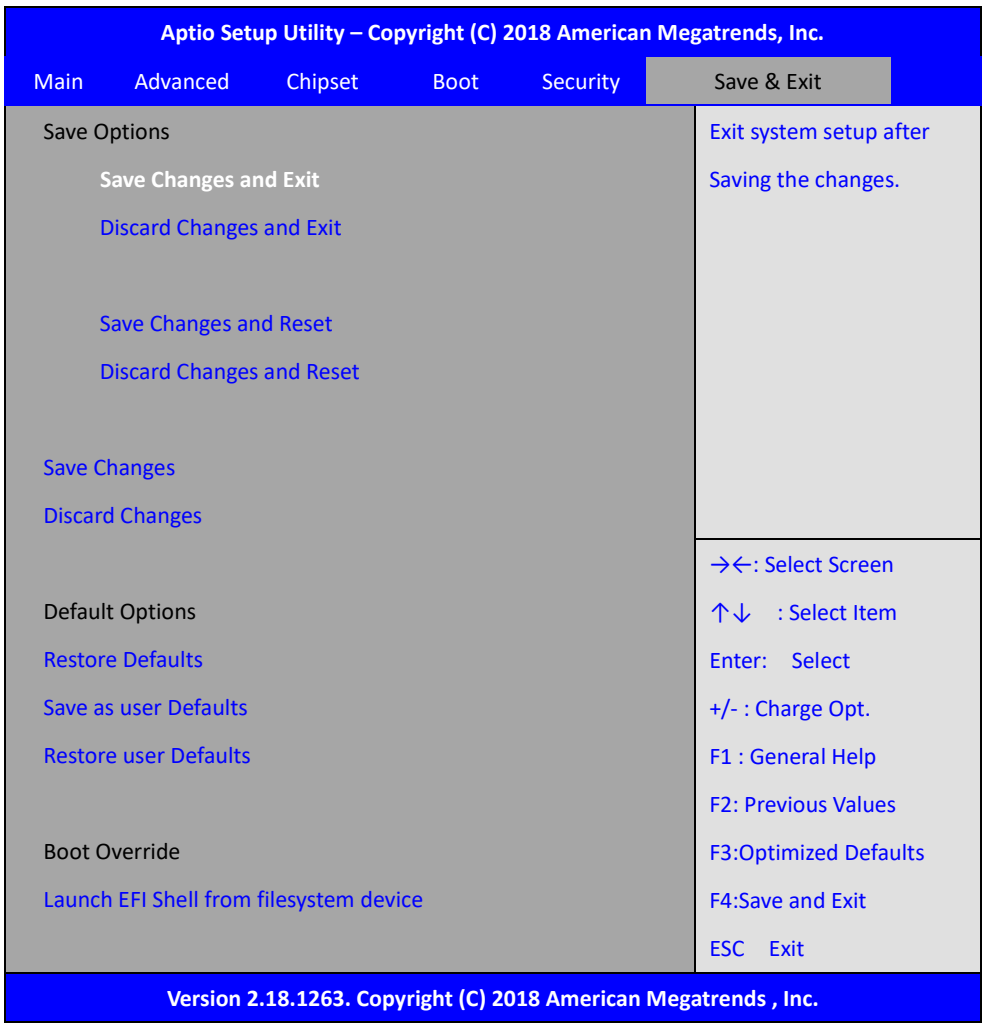
►Save all Secure Boot variables

Secure Boot variables	**Size**	**Key#**	**Key Source**
►Platform Key(PK)	**0**	**0**	**No Key**
► Key Exchange Keys	**0**	**0**	**No Key**
► Authorized Signatures	**0**	**0**	**No Key**
►Forbidden Signatures	**0**	**0**	**No Key**
► Authorized TimeStamps	**0**	**0**	**No Key**
► osRecovery Signatures	**0**	**0**	**No Key**

3.7 Boot Settings

Setup Prompt Timeout	1
Bootup Numlock State	**[On]**
Quiet Boot	**[Disabled]**
Boot Option Priorities	
Fast Boot	**[Disabled]**
New Boot Option Policy	**[Default]**

3.8 Save & Exit Settings



Save Changes and Exit

Save & Exit Setup save Configuration and exit ?

[Yes]

[No]

Discard Changes and Ext

Exit without Saving Quit without saving?

[Yes]

[No]

Save Changes

Save configuration?

[Yes]

[No]

Discard Changes

Load Previous Values?

[Yes]

[No]

Default Options

Restore Default

Load Optimized Defaults?

[Yes]

[No]

Save User Default

Save configuration?

[Yes]

[No]

Restore User Default

Restore User Default?

[Yes]

[No]

Boot Override

Launch EFI Shell from filesystem device

WARNING Not Found

[ok]

Chapter 4 Installation of Drivers

This chapter describes the installation procedures for software and drivers under Windows 8.1 & 10. The software and drivers are included with the motherboard. The contents include **Intel H170, Graphics 530 chipset driver, Audio driver, Intel® management engine interface, and DPTF Driver Installation instructions are given below.**

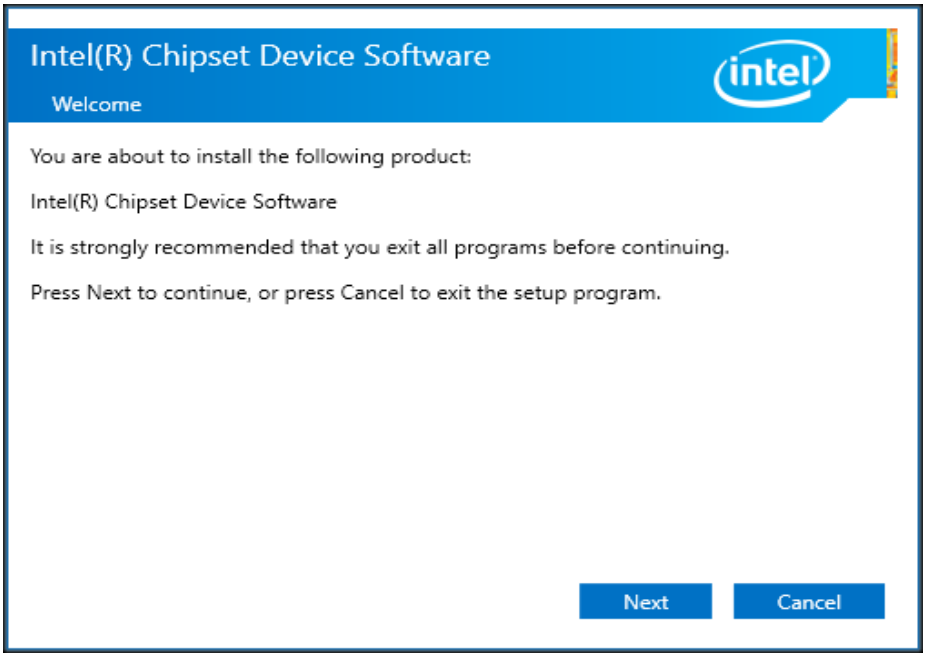
Important Note:
After installing your Windows operating system, you must install Intel Chipset Software Installation Utility before proceeding with the installation of drivers.

4.1 Intel H170 Chipset

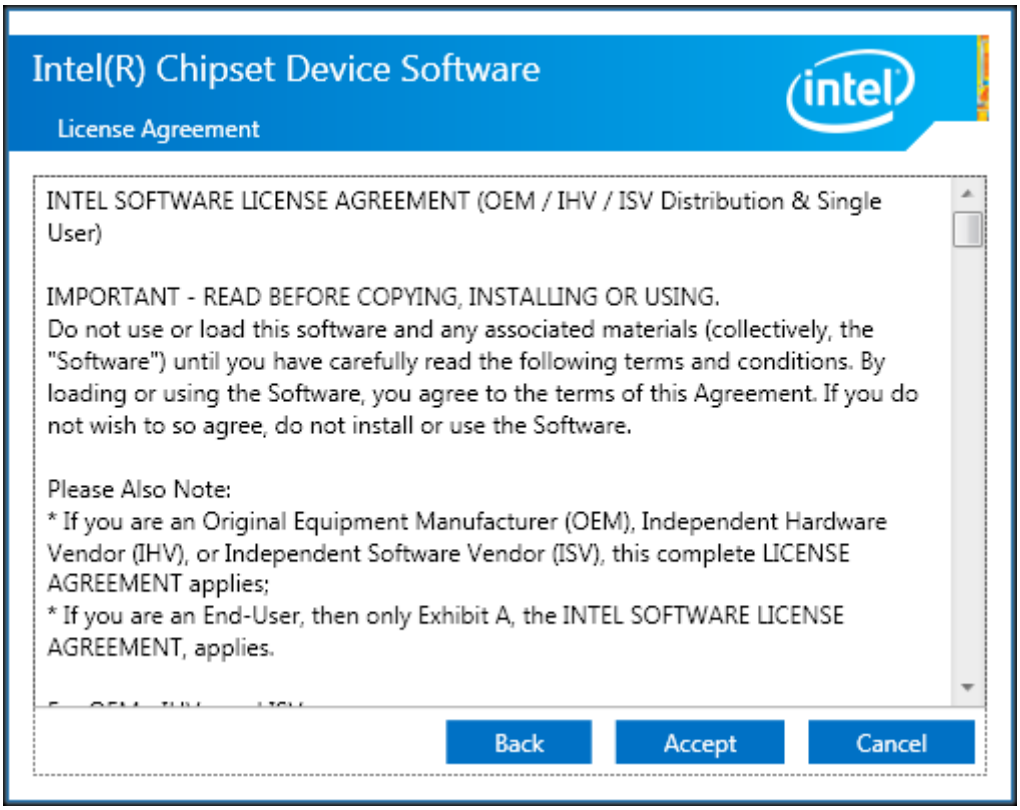
To install the Intel H170chipset driver, please follow the steps below.

Step1. Select **Intel H170 Chipset** from the list

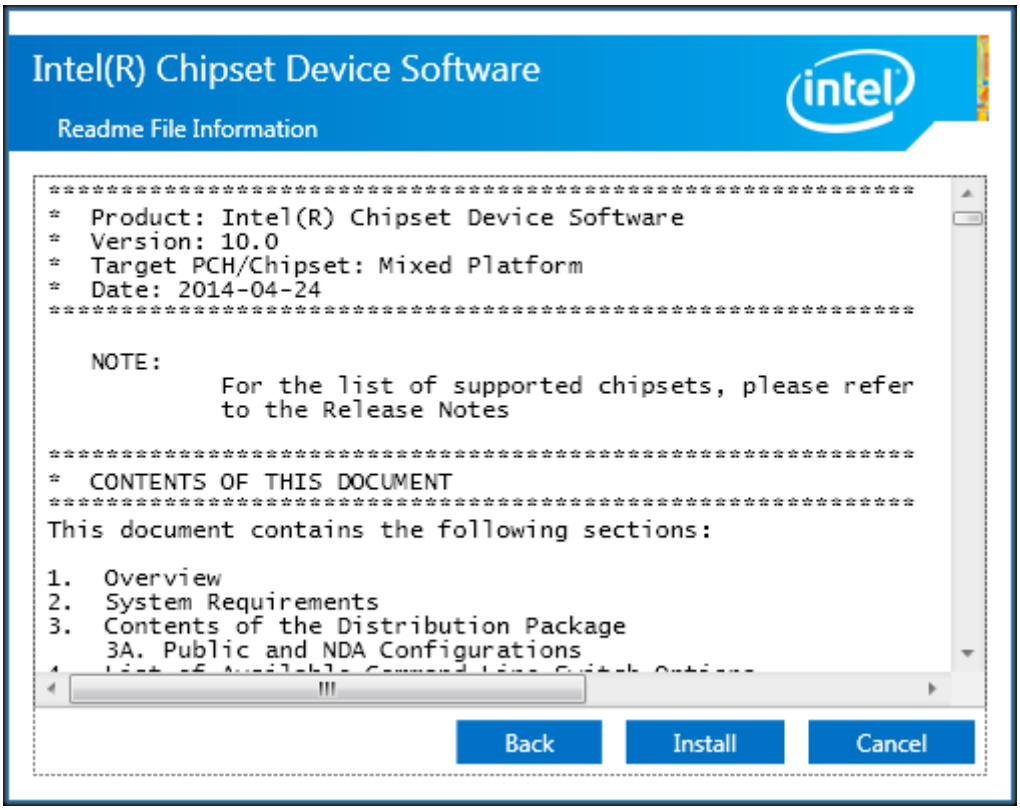
Step2. Click **Next** to setup program.



Step3. Read the license agreement. Click **Accept** to accept all of the terms of the license agreement.



Step4. Click **Install** to begin the installation.



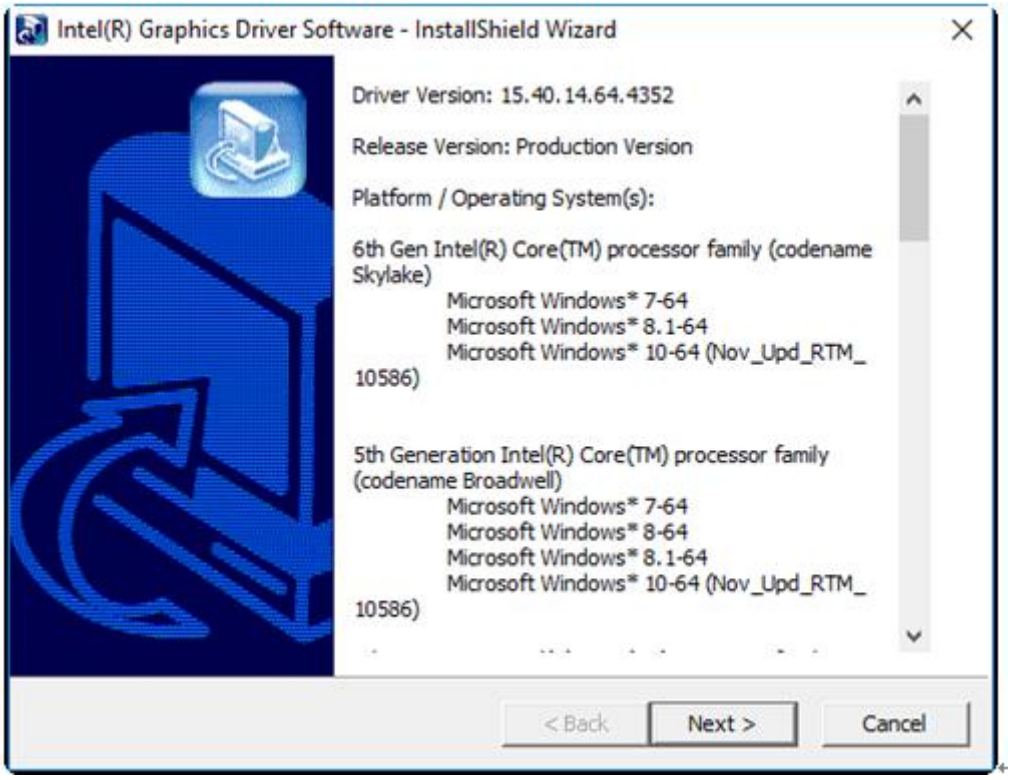
Step5. Click **Finish** to complete the setup process.

4.2 Intel® HD Graphics 530 Chipset

To install the Intel® HD Graphics 530 Chipset, please follow the steps below.

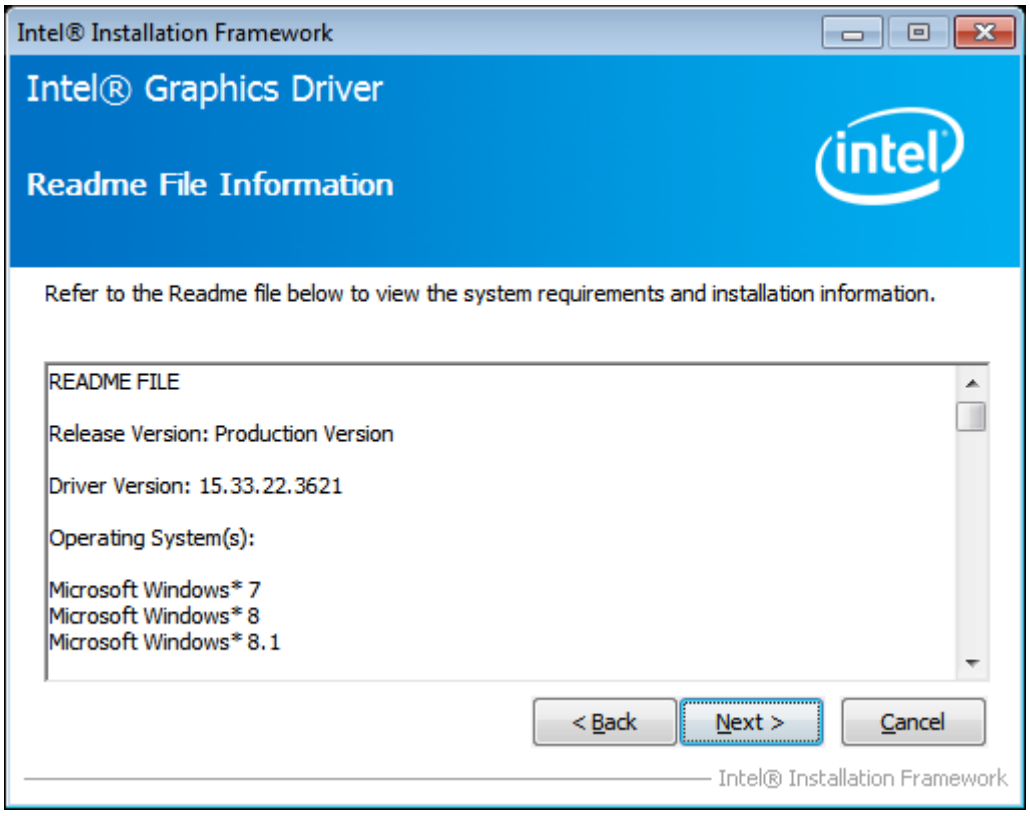
Step1. Select **Intel® HD Graphics 530 Chipset** from the list**.**

Step2. Click **Next.**

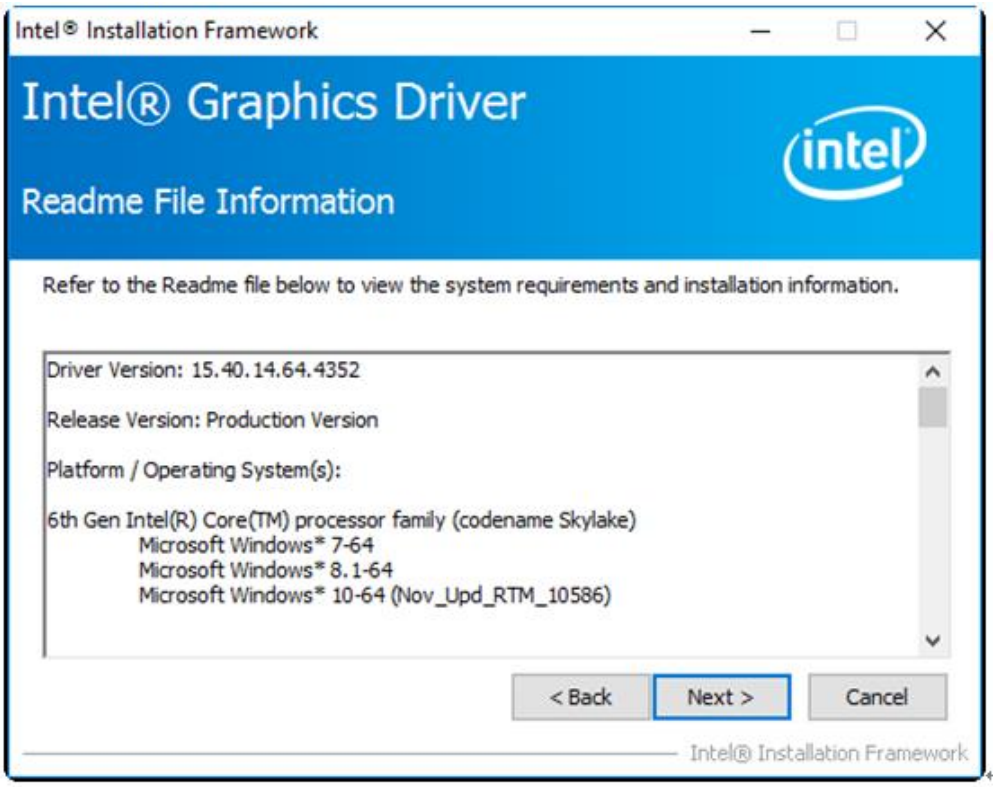


Step3. Choose **automatically run** function and Click **Next** to setup program.

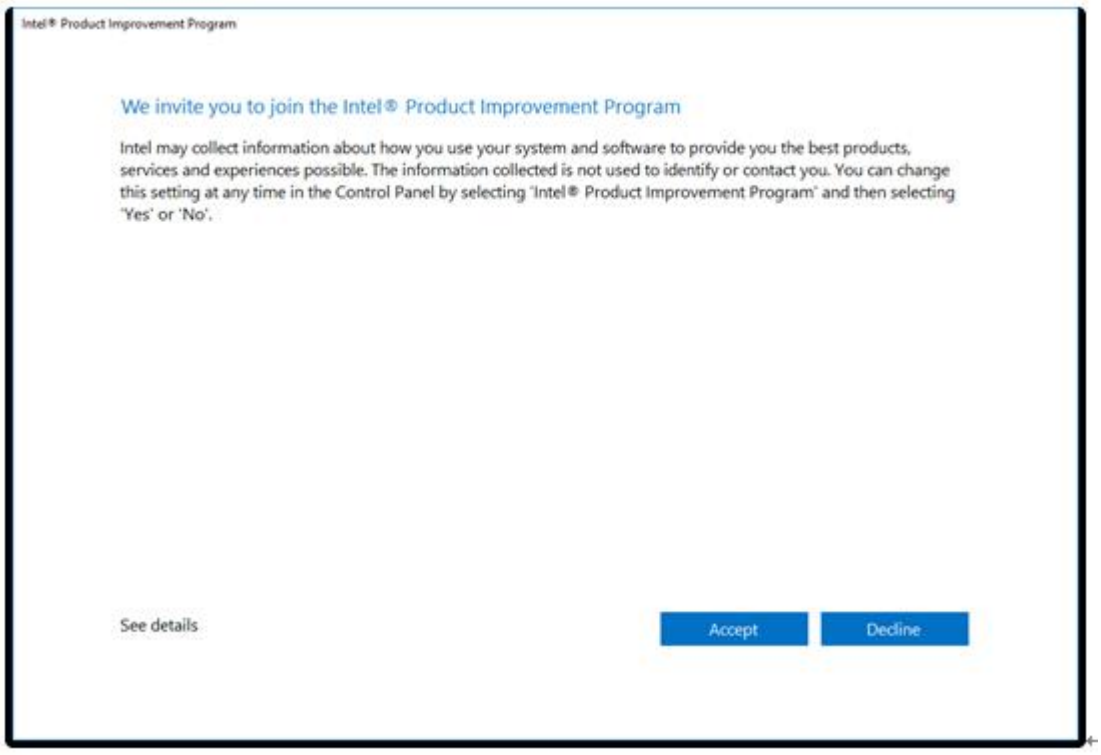
Step4. Read the license agreement. Click **Yes** to accept all of the terms of the license agreement.



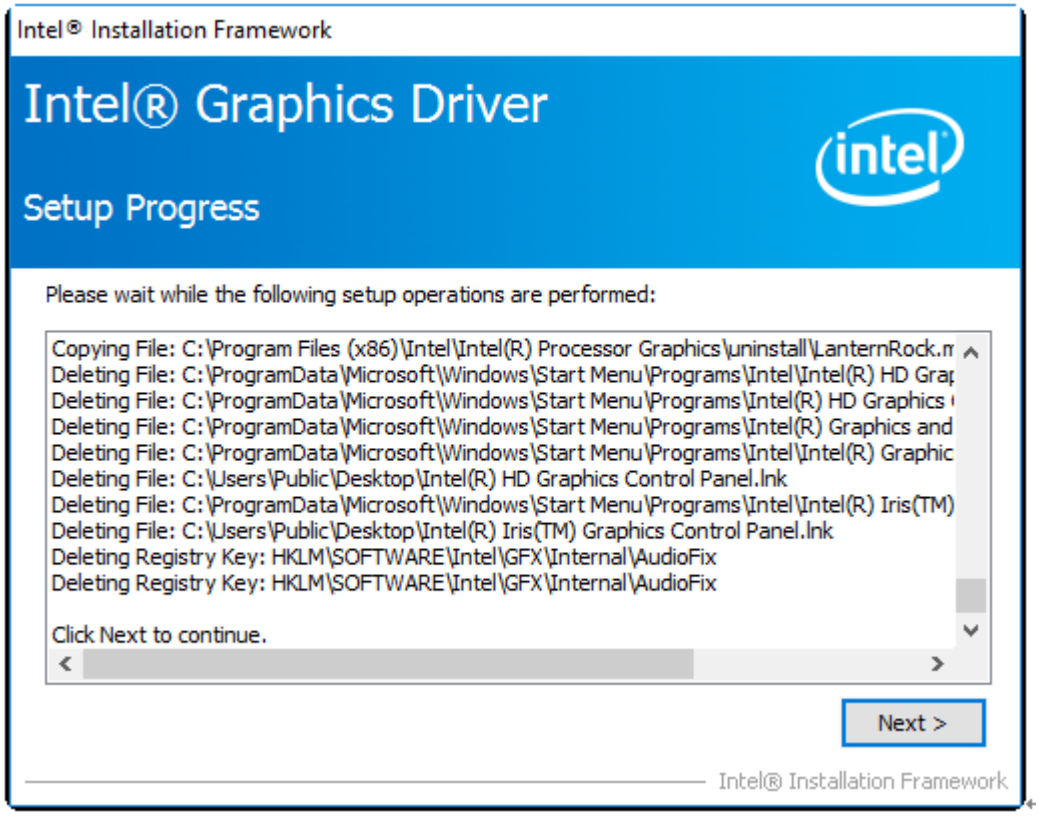
Step5. Click **Next** to continue.



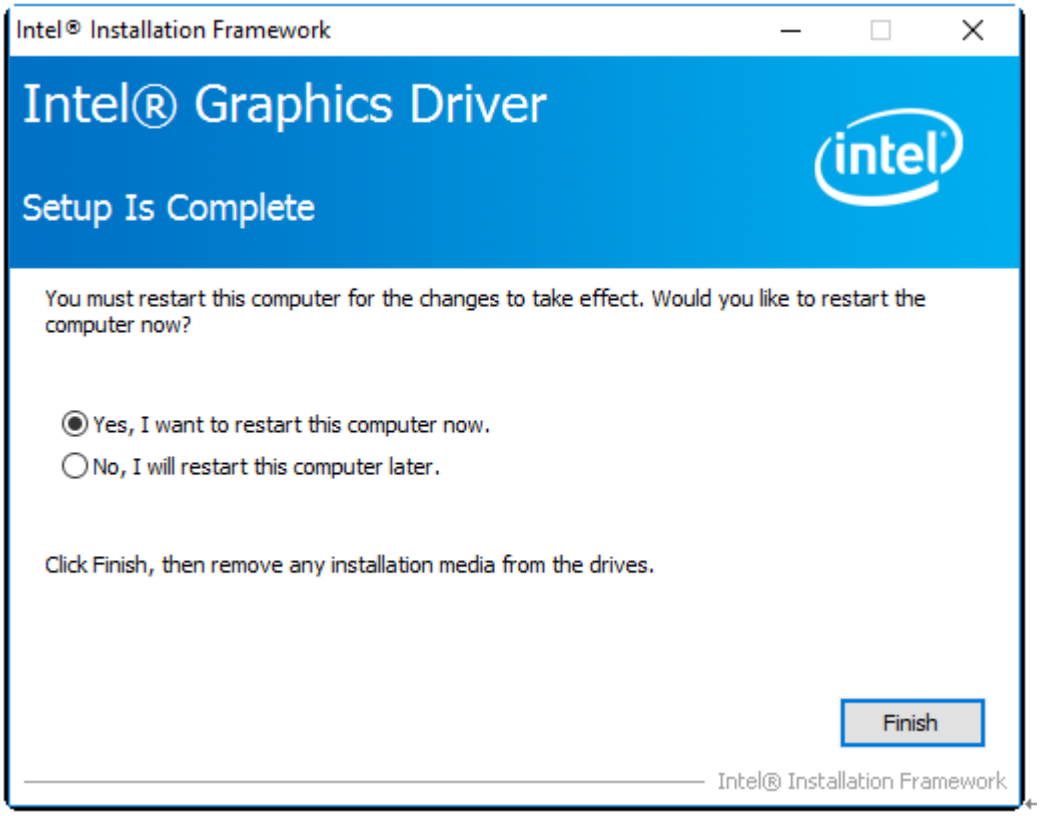
Step6. Here is Intel product improvement program information, you can choose **Accept** or **Decline** by your option and installation will go to next step.



Step7. Click **Next** to continue the program.



Step8. Select **Yes, I want to restart this computer now**. Click **Finish** to complete installation.

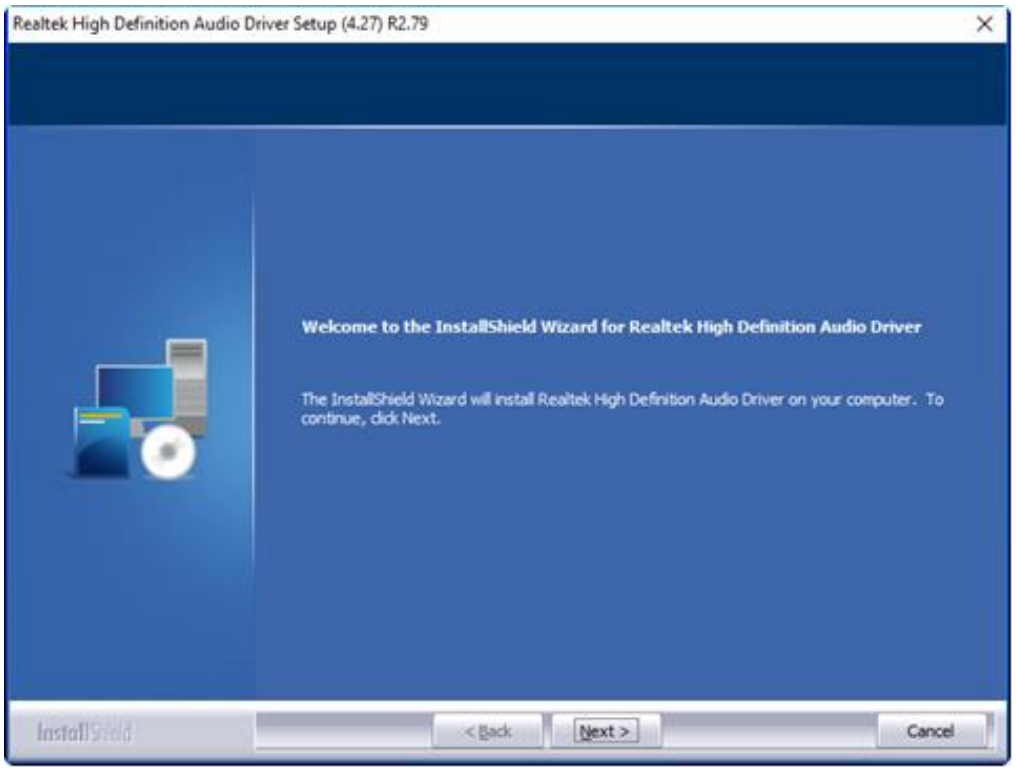


4.3 Realtek ALC269 HD Audio Driver Installation

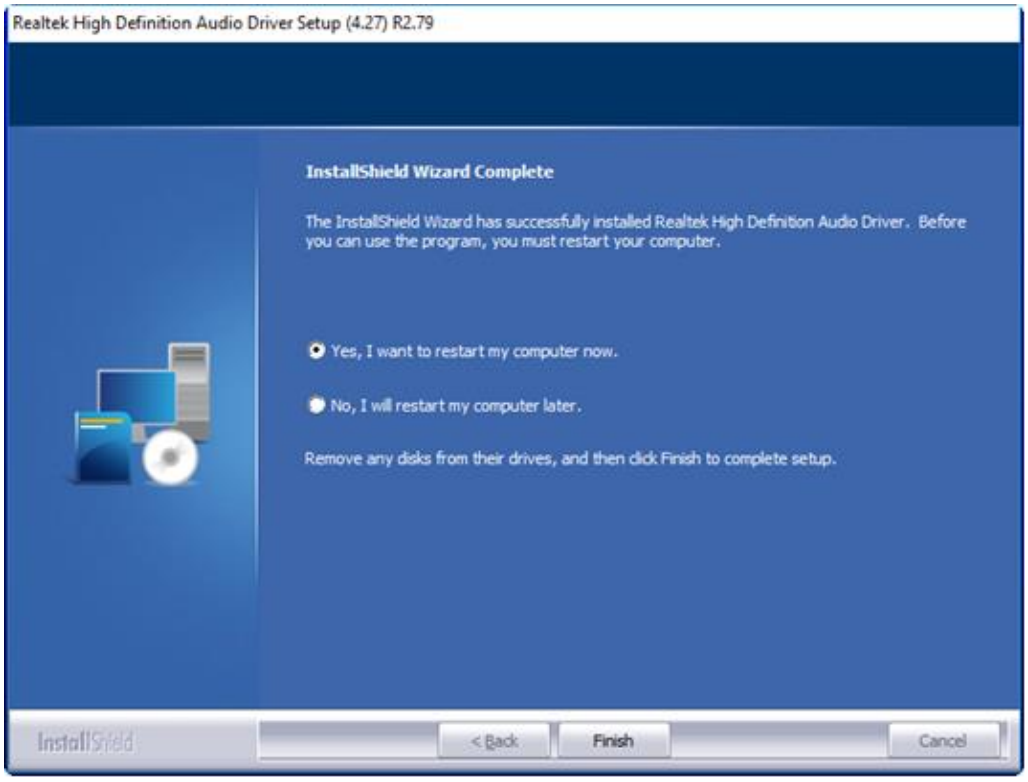
To install Realtek ALC269 HD Audio Driver, please follow the steps below.

Step1. Select **Realtek AL269 HD Audio Driver** from the list**.**

Step2. Click **Next** to continue.



Step3. Click **Yes, I want to restart my computer now**. Click **Finish** to complete the installation.

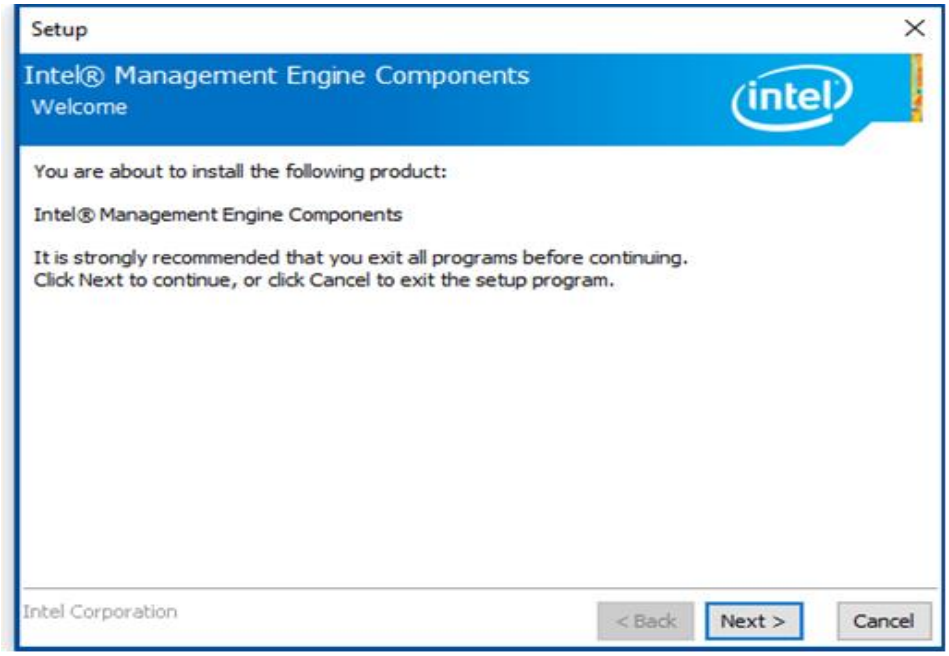


4.4 Intel® Management Engine Interface

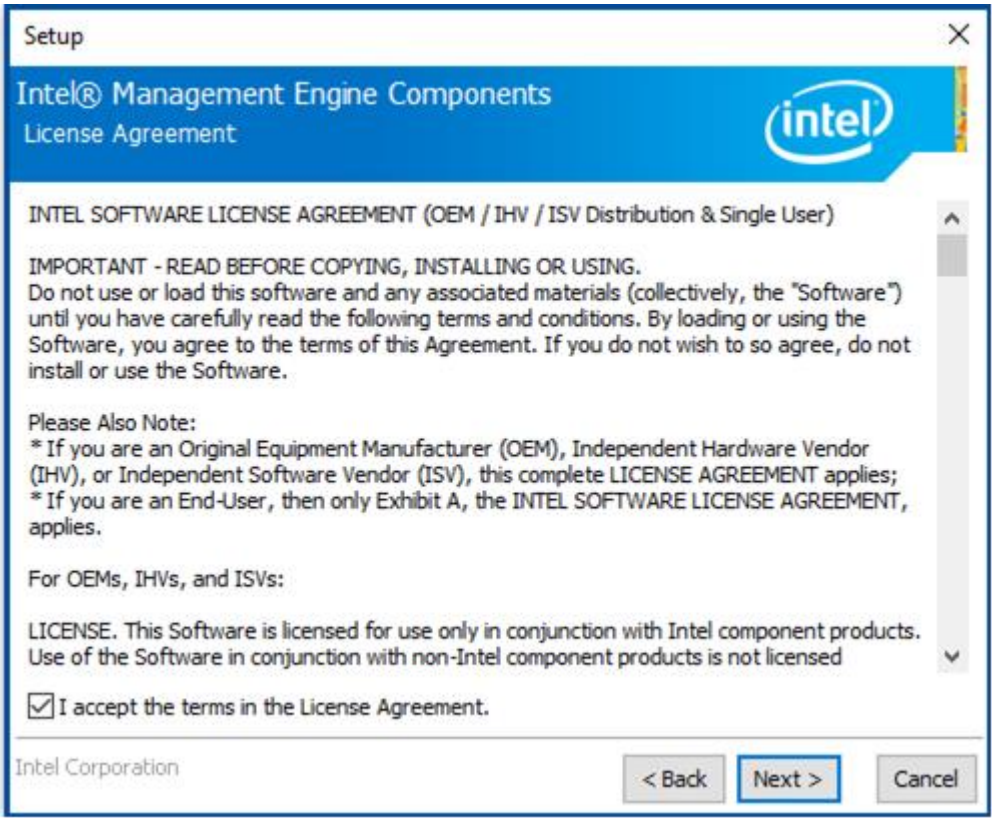
To install the Intel® Management Engine Interface, please follow the steps below.

Step1. Select **Intel® Management Engine Interface** from the list

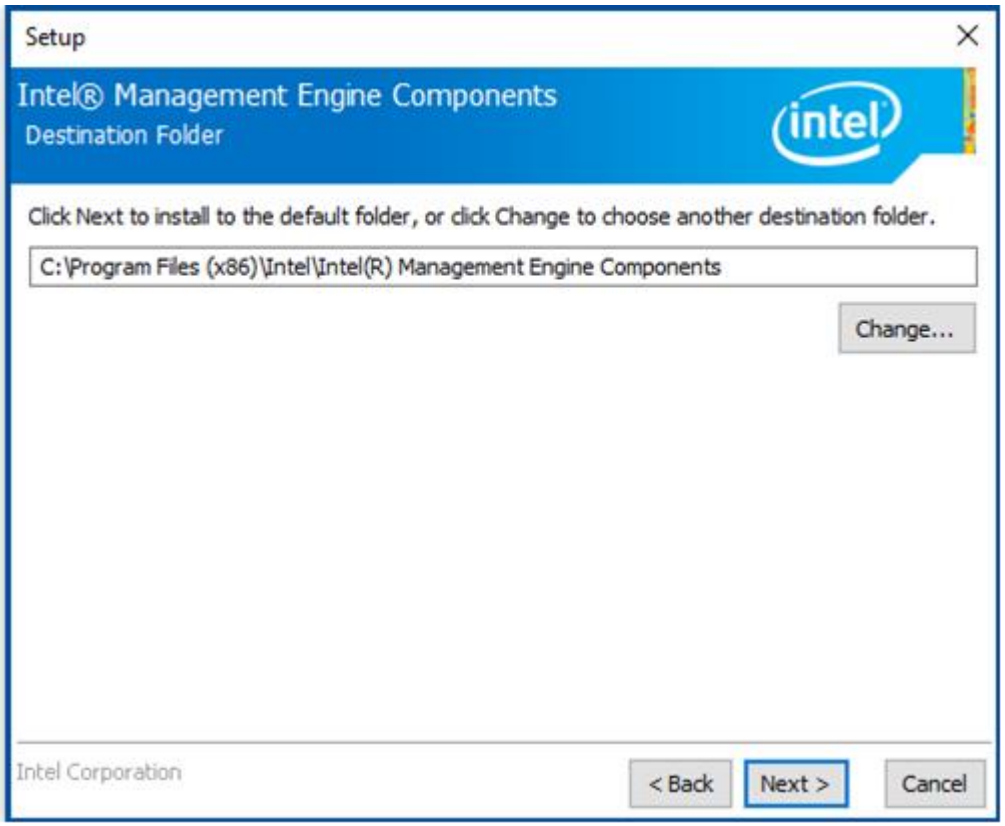
Step2. Select setup language you need. Click **Next** to continue.



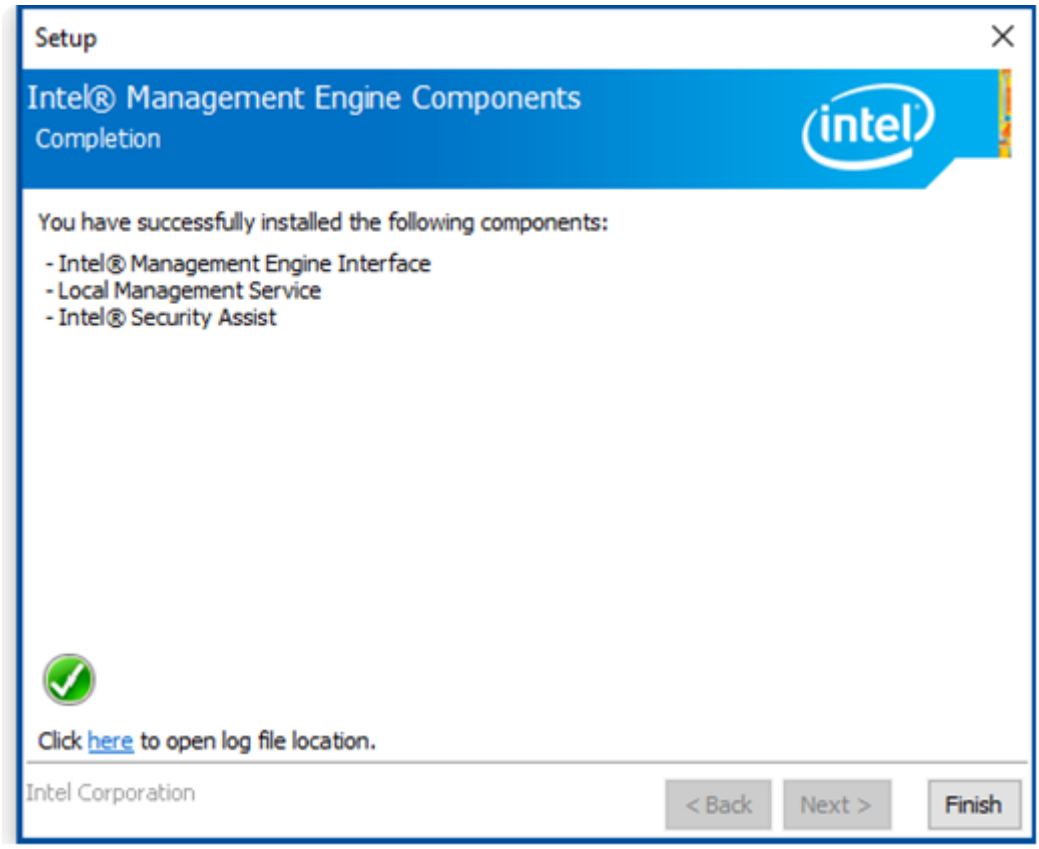
Step3. Choose **I accept the terms in the License Agreement** and click **Next** to begin the installation.



Step4. Click **Next** to continue.



Step5. Click **Finish** to complete the installation.



Chapter 5 Mounting Suggestions

5.1 Din Rail Mount

5.1.1 TB-5545-MVS Din Rail Mount

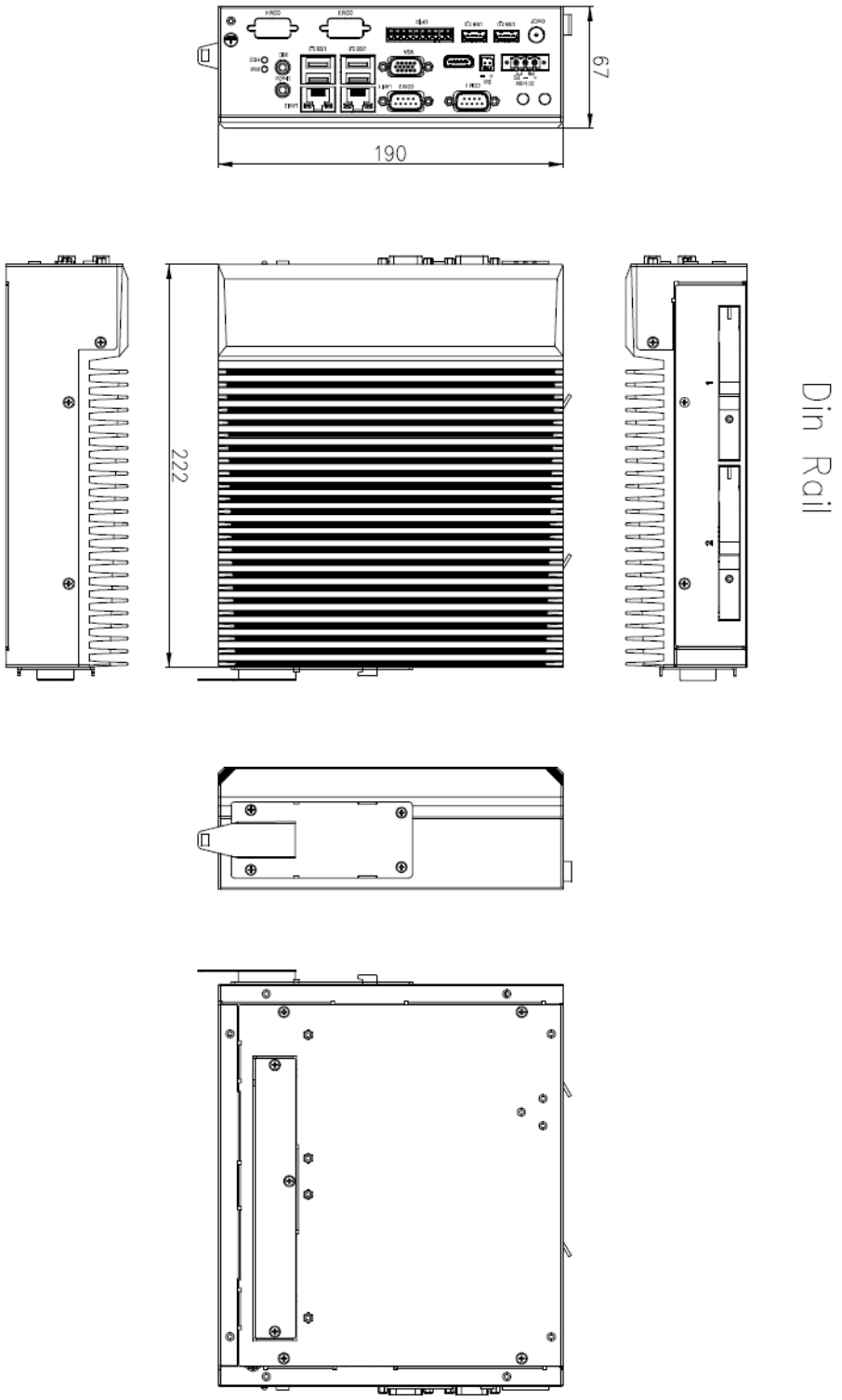


Figure 5.1 Din Rail Mount of TB-5545-MVS

5.1.2 TB-5545-MVS x2 expansion Din Rail Mount

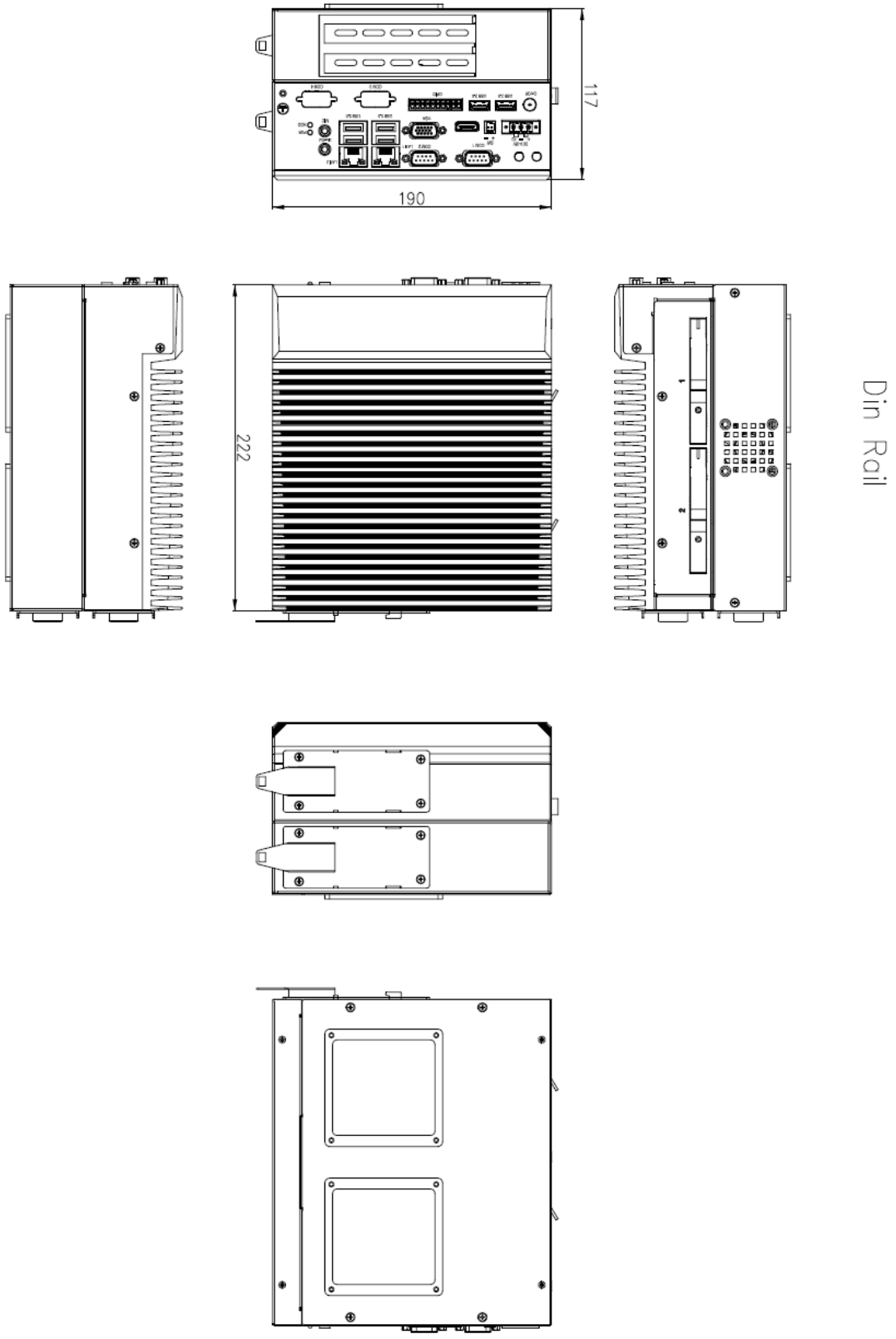


Figure 5.2 Din Rail Mount of TB-5545-MVS x2 expansion

5.1.3 TB-5545-MVS x4 expansion Din Rail Mount

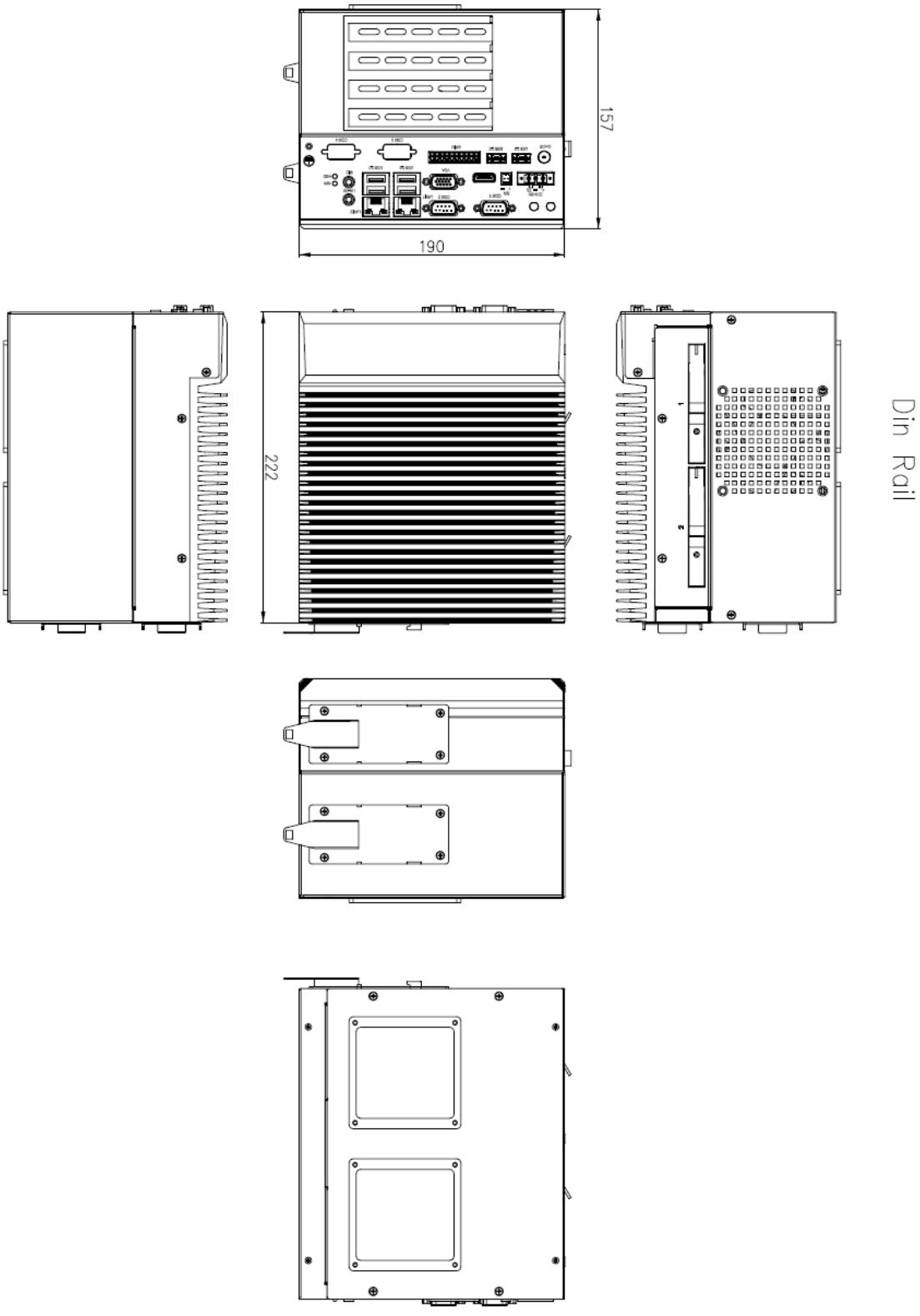


Figure 5.3 Din Rail Mount of TB-5545-MVS x4 expansion

5.2 Wall Mount

5.2.1 TB-5545-MVS Wall Mount

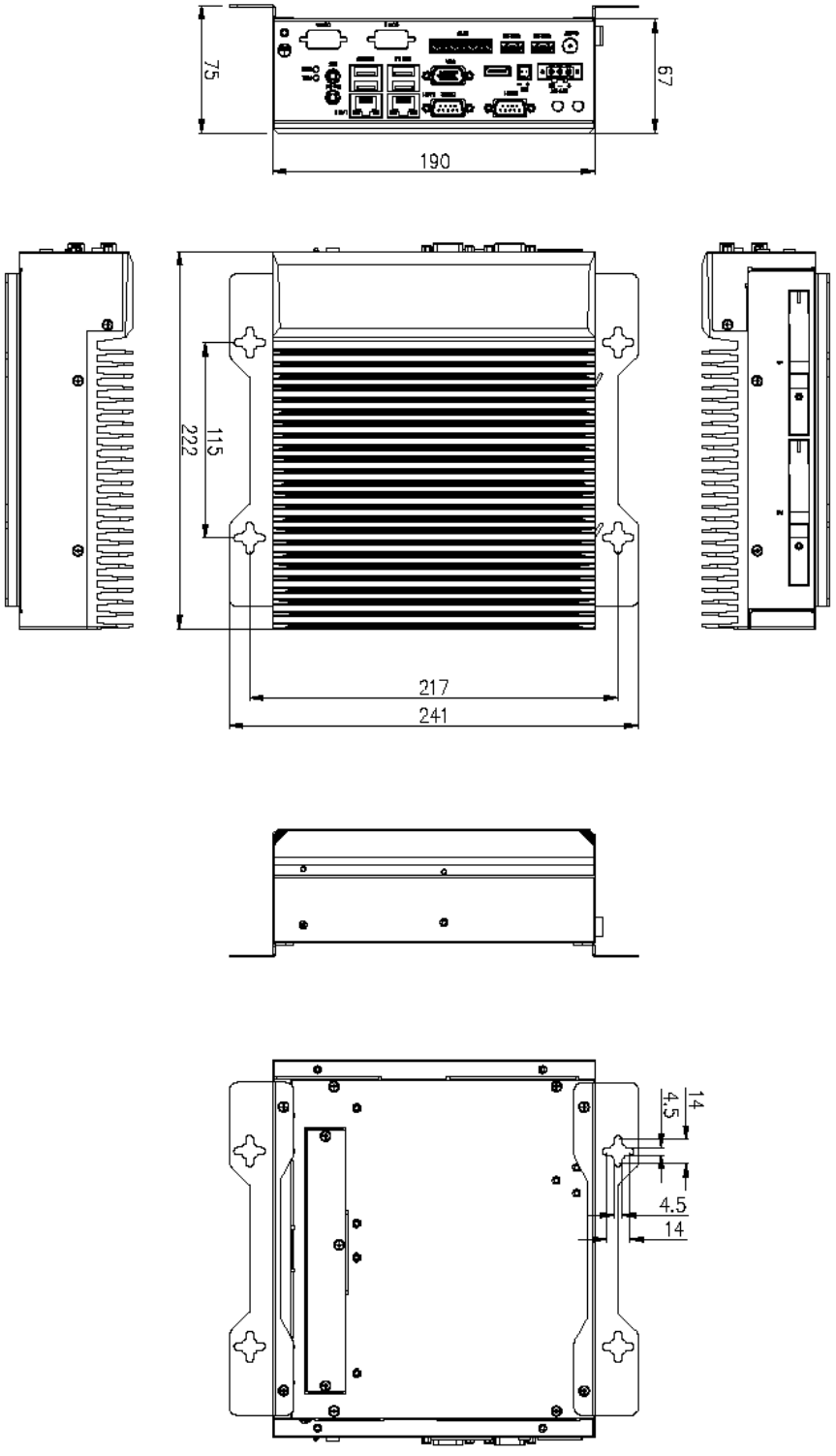


Figure 5.4 Wall Mount of TB-5545-MVS

5.2.2 TB-5545-MVS x2 expansion Wall Mount

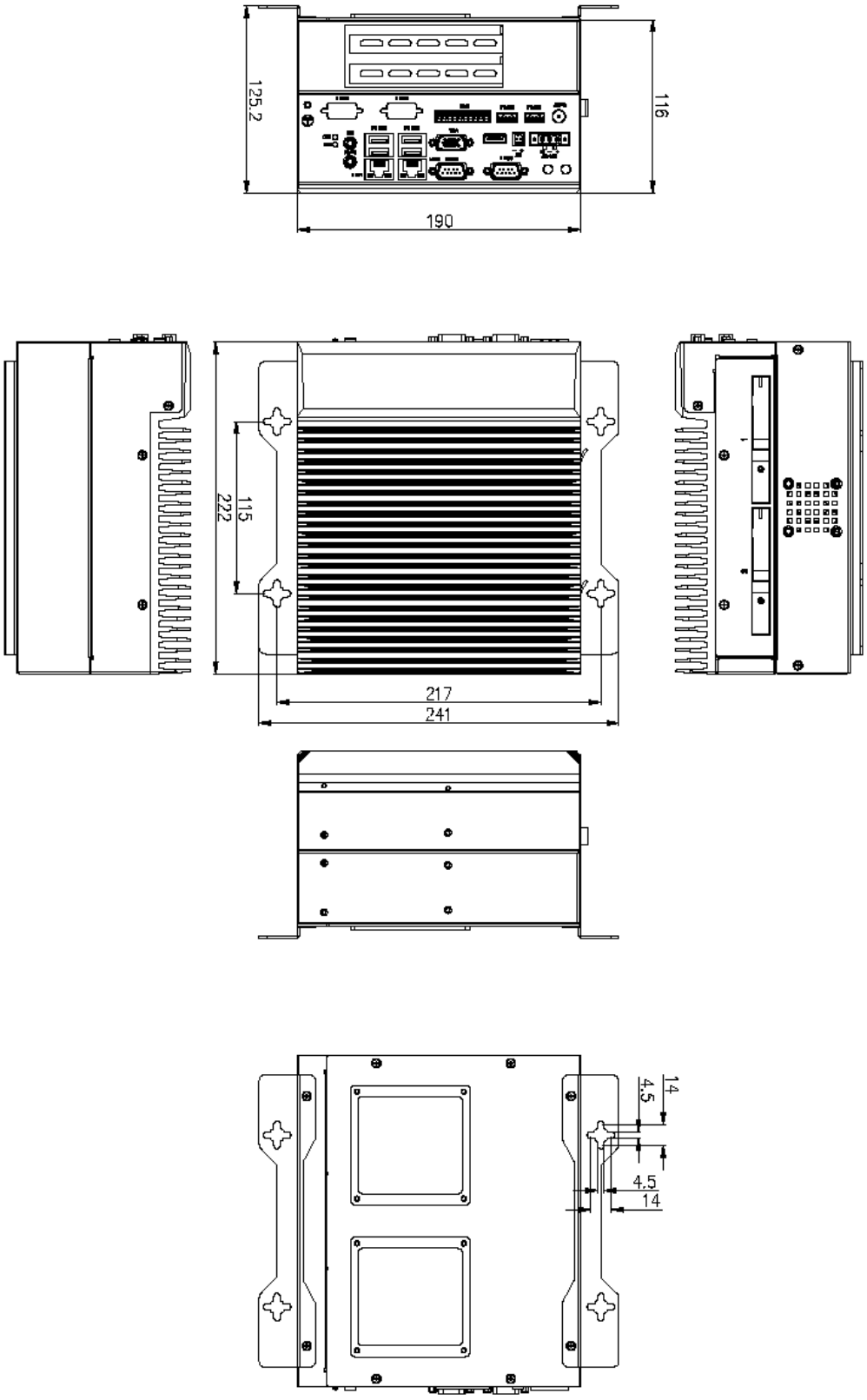


Figure 5.5 Wall Mount of TB-5545-MVS x2 expansion

5.2.3 TB-5545-MVS x4 expansion Wall Mount

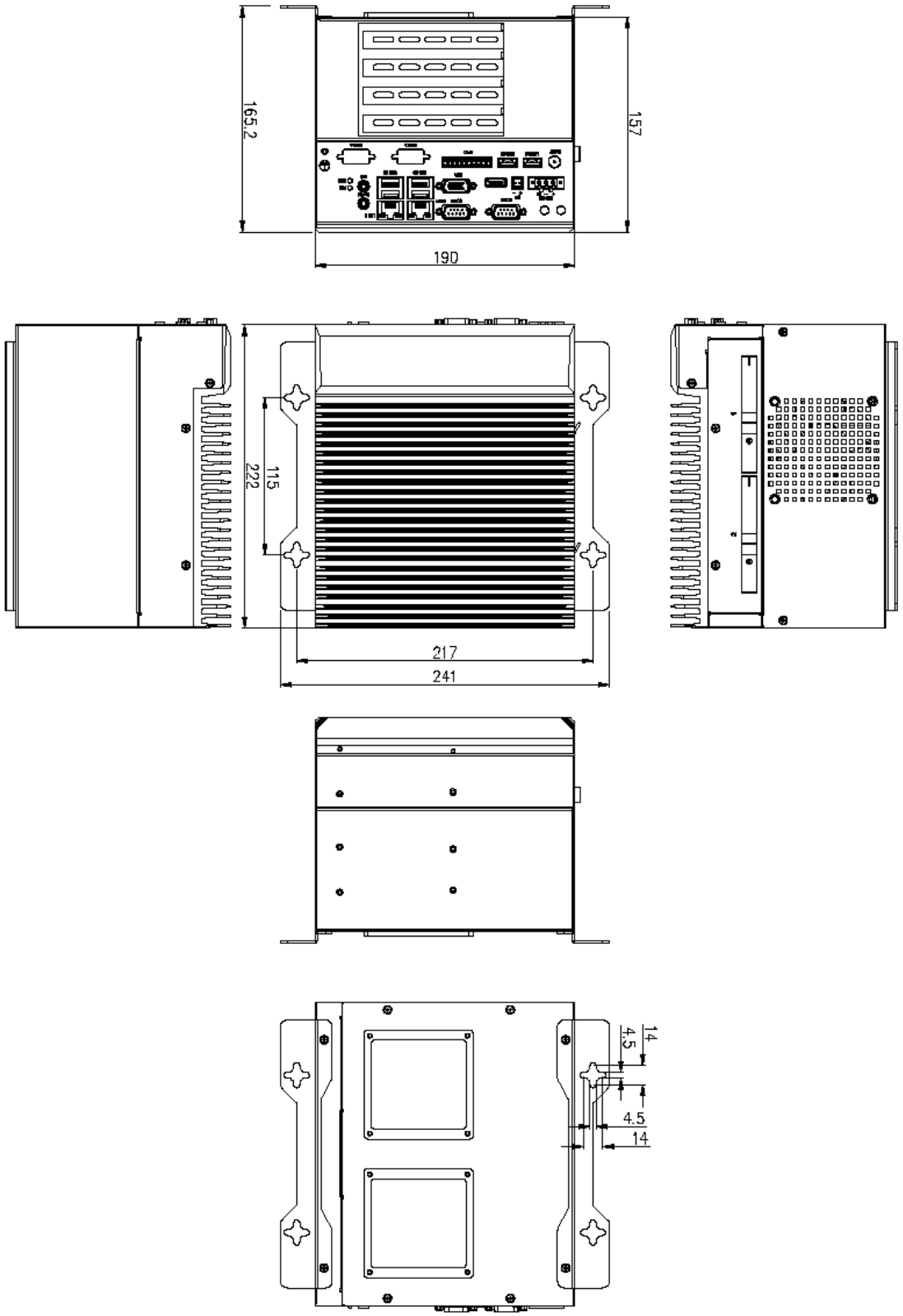


Figure 5.6 Wall Mount of TB-5545-MVS x4 expansion