Rambus

MIPI IP Core Size & Speed
ASIC & FPGA

To The Point Solutions

Version 4.63

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Introduction

Rambus provides a broad range of high-performance, easy-to-use IP Cores. This document summarizes the speed and size for each of these cores for a variety of devices.

It is important to note that the speed and size are “typical maximum” values. The actual speed and size is dependent on a wide variety of factors including:

- Device speed grade
- Device size
- Bus loading
- Pin selection
- Internal routing
- Exact configuration of the core
- Use of hard-coded versus soft-coded parameters

Contact Rambus to review your overall design requirements and receive a more specific core speed and size for your design.

For more information on Rambus and our IP Cores:

- Visit our website at www.rambus.com
- Send an e-mail to rcg@rambus.com

CSI-2 Controller Core V2

Device	Version	Data Rate (per lane)	Internal Clock Rate	Size With D-PHY Support	Size With D/C-PHY Support
ASIC	32 Bit Core Width Transmitter	D-PHY: 2,500+ Mbit/s	D-PHY: 312.5+ MHz	15,000 Gates 0 Bits RAM	16,000 Gates 0 Bits RAM
ASIC	32 bit Core Width Receiver	D-PHY: 2,500+ Mbit/s	D-PHY: 312.5+ MHz	14,000 Gates 512 Bits RAM	22,000 Gates 512 Bits RAM
ASIC	64 Bit Core Width Transmitter	D-PHY: 2,500+ Mbit/s C-PHY: 2,500+ Msym/s	D-PHY: 312.5+ MHz C-PHY: 356.25+ MHz	27,000 Gates 0 Bits RAM	28,000 Gates 0 Bits RAM
ASIC	64 Bit Core Width Receiver	D-PHY: 2,500+ Mbit/s C-PHY: 2,500+ Msym/s	D-PHY: 312.5+ MHz C-PHY: 356.25+ MHz	25,000 Gates 1024 Bits RAM	33,000 Gates 1024 Bits RAM

Notes:

1. 32 bit core width supports 1-4 D-PHY lanes, 1-2 lanes (trios)
2. 64 bit core width supports 1-8 D-PHY lanes, 1-4 C-PHY lanes (trios)

DSI-2 Controller Core

Device	Version	Data Rate (per lane)	Internal Clock Rate	Size With D-PHY Support	Size With D/C-PHY Support
ASIC	32 Bit Core Width Host	D-PHY: 2,500+ Mbit/s	D-PHY: 312.5+ MHz	15,000 Gates 0 Bits RAM	16,000 Gates 0 Bits RAM
ASIC	32 bit Core Width Peripheral	D-PHY: 2,500+ Mbit/s	D-PHY: 312.5+ MHz	20,000 Gates 512 Bits RAM	27,000 Gates 512 Bits RAM
ASIC	64 Bit Core Width Host	D-PHY: 2,500+ Mbit/s C-PHY: 2,500+ Msym/s	D-PHY: 312.5+ MHz C-PHY: 356.25+ MHz	16,000 Gates 0 Bits RAM	17,000 Gates 0 Bits RAM
ASIC	64 Bit Width Peripheral	D-PHY: 2,500+ Mbit/s C-PHY: 2,500+ Msym/s	D-PHY: 312.5+ MHz C-PHY: 356.25+ MHz	24,000 Gates 1024 Bits RAM	31,000 Gates 1024 Bits RAM

Notes:

1. 32 bit core width supports 1-4 D-PHY lanes, 1-2 C-PHY lanes (trios)
2. 64 bit core width supports 1-4 D-PHY lanes, 1-4 C-PHY lanes (trios)

CSI-2 Controller Core V2 (32 Bit)

Device	Version	Data Rate (per lane)	Clock Rate	Size
Stratix 10	Transmitter	1,500 Mbit/s	187 MHz	1,200 ALUTs, 0 M20K RAMs
	Receiver	1,500 Mbit/s	187 MHz	1,600 ALUTs, 4 M20K RAMs
Stratix V	Transmitter	1,500 Mbit/s	187 MHz	1,200 ALUTs, 0 M20K RAMs
	Receiver	1,500 Mbit/s	187 MHz	1,600 ALUTs, 4 M20K RAMs
Stratix IV	Transmitter	1,400 Mbit/s	175 MHz	1,200 ALUTs, 0 M20K RAMs
	Receiver	1,400 Mbit/s	175 MHz	1,600 ALUTs, 4 M20K RAMs
Arria 10	Transmitter	1,500 Mbit/s	187 MHz	1,200 ALUTs, 0 M20K RAMs
	Receiver	1,500 Mbit/s	187 MHz	1,600 ALUTs, 4 M20K RAMs
Arria V	Transmitter	1,250 Mbit/s	156 MHz	1,200 ALUTs, 0 M10K RAMs
	Receiver	1,250 Mbit/s	156 MHz	1,600 ALUTs, 4 M10K RAMs
Cyclone V	Transmitter	840 Mbit/s	105 MHz	1,200 ALUTs, 0 M10K RAMs
	Receiver	840 Mbit/s	105 MHz	1,600 ALUTs, 4 M10K RAMs
Cyclone IV	Transmitter	840 Mbit/s	105 MHz	2,140 LEs, 0 M9K RAMs
	Receiver	840 Mbit/s	105 MHz	2,900 LEs, 4 M9K RAMs
MAX 10	Transmitter	720 Mbit/s	90 MHz	2,140 LEs, 0 M9K RAMs
	Receiver	720 Mbit/s	90 MHz	2,900 LEs, 4 M9K RAMs

Notes:

1. Data Rate limited to 1,500 Mbit/s per MIPI specification even if device supports faster LVDS rates
2. Clock Rate 1/8th of Data Rate
3. 4 D-PHY lane implementation

DSI-2 Controller Core (32 Bit)

Device	Version	Data Rate (per lane)	Clock Rate	Size
Stratix 10	Host	1,500 Mbit/s	187 MHz	1140 ALUTs, 0 M20K RAMs
	Peripheral	1,500 Mbit/s	187 MHz	1520 ALUTs, 4 M20K RAMs
Stratix V	Host	1,500 Mbit/s	187 MHz	1140 ALUTs, 0 M20K RAMs
	Peripheral	1,500 Mbit/s	187 MHz	1520 ALUTs, 4 M20K RAMs
Stratix IV	Host	1,400 Mbit/s	175 MHz	1140 ALUTs, 0 M20K RAMs
	Peripheral	1,400 Mbit/s	175 MHz	1520 ALUTs, 4 M20K RAMs
Arria 10	Host	1,500 Mbit/s	187 MHz	1140 ALUTs, 0 M20K RAMs
	Peripheral	1,500 Mbit/s	187 MHz	1520 ALUTs, 4 M20K RAMs
Arria V	Host	1,250 Mbit/s	156 MHz	1140 ALUTs, 0 M10K RAMs
	Peripheral	1,250 Mbit/s	156 MHz	1520 ALUTs, 4 M10K RAMs
Cyclone V	Host	840 Mbit/s	105 MHz	1140 ALUTs, 0 M10K RAMs
	Peripheral	840 Mbit/s	105 MHz	1520 ALUTs, 4 M10K RAMs
Cyclone IV	Host	840 Mbit/s	105 MHz	2052 LEs, 0 M9K RAMs
	Peripheral	840 Mbit/s	105 MHz	2736 LEs, 4 M9K RAMs
MAX 10	Host	720 Mbit/s	90 MHz	2052 LEs, 0 M9K RAMs
	Peripheral	720 Mbit/s	90 MHz	2736 LEs, 4 M9K RAMs

Notes:

1. Data Rate limited to 1,500 Mbit/s per MIPI specification even if device supports faster LVDS rates
2. Clock Rate 1/8th of Data Rate
3. 4 D-PHY lane implementation

CSI-2 Controller Core V2 (32 bit)

Device	Version	Data Rate (per lane)	Internal Clock Rate	Size
Virtex UltraScale+ Kintex UltraScale+ Zynq UltraScale+	Transmitter	1,500 Mbit/s	187 MHz	1,620 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	1,800 LUT6s
Virtex UltraScale Kintex UltraScale Zynq UltraScale	Transmitter	1,250 Mbit/s	156 MHz	1,620 LUT6s
	Receiver	1,250 Mbit/s	156 MHz	1,800 LUT6s
Virtex-7	Transmitter	1,500 Mbit/s	187 MHz	1,620 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	1,800 LUT6s
Zynq-7000 Kintex-7	Transmitter	1,500 Mbit/s	187 MHz	1,620 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	1,800 LUT6s
Zynq-7000 Artix-7	Transmitter	1,250 Mbit/s	156 MHz	1,620 LUT6s
	Receiver	1,250 Mbit/s	156 MHz	1,800 LUT6s
Spartan-6	Transmitter	1,080 Mbit/s	135 MHz	1,620 LUT6s
	Receiver	1,080 Mbit/s	135 MHz	1,800 LUT6s

Notes:

1. Assumes the use of the HP I/O. Contact Rambus for supported HR I/O rates
2. Zynq-7000 devices are either Kintex-7 or Artix-7 fabric based
3. Data Rate limited to 1,500 Mbit/s per MIPI specification even if device supports faster LVDS rates
4. Clock Rate 1/8th of Data Rate
5. 4 D-PHY lane implementation
6. Support of LogiCORE D-PHY data rates up to 2,500 Mbit/s per lane available with Kintex Ultrascale+ or Zynq Ultrascale+

CSI-2 Controller Core V2 (64 bit)

Device	Version	Data Rate (per lane)	Internal Clock Rate	Size
Virtex UltraScale+ Kintex UltraScale+ Zynq UltraScale+	Transmitter	1,500 Mbit/s	187 MHz	3,800 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	3,600 LUT6s
Virtex UltraScale Kintex UltraScale Zynq UltraScale	Transmitter	1,250 Mbit/s	156 MHz	3,800 LUT6s
	Receiver	1,250 Mbit/s	156 MHz	3,600 LUT6s
Virtex-7	Transmitter	1,500 Mbit/s	187 MHz	3,800 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	3,600 LUT6s
Zynq-7000 Kintex-7	Transmitter	1,500 Mbit/s	187 MHz	3,800 LUT6s
	Receiver	1,500 Mbit/s	187 MHz	3,600 LUT6s
Zynq-7000 Artix-7	Transmitter	1,250 Mbit/s	156 MHz	3,800 LUT6s
	Receiver	1,250 Mbit/s	156 MHz	3,600 LUT6s
Spartan-6	Transmitter	1,080 Mbit/s	135 MHz	3,800 LUT6s
	Receiver	1,080 Mbit/s	135 MHz	3,600 LUT6s

Notes:

1. Assumes the use of the HP I/O. Contact Rambus for supported HR I/O rates
2. Zynq-7000 devices are either Kintex-7 or Artix-7 fabric based
3. Data Rate limited to 1,500 Mbit/s per MIPI specification even if device supports faster LVDS rates
4. Clock Rate 1/8th of Data Rate
5. 8 D-PHY lane implementation
6. Support of LogiCORE D-PHY data rates up to 2,500 Mbit/s per lane available with Kintex Ultrascale+ or Zynq Ultrascale+

DSI-2 Controller Core (32 Bit)

Device	Version	Data Rate (per lane)	Clock Rate	Size
Virtex UltraScale+ Kintex UltraScale+ Zynq UltraScale+	Host	1,500 Mbit/s	187 MHz	1200 LUT6s
	Peripheral	1,500 Mbit/s	187 MHz	1600 LUT6s
Virtex UltraScale Kintex UltraScale Zynq UltraScale	Host	1,250 Mbit/s	156 MHz	1200 LUT6s
	Peripheral	1,250 Mbit/s	156 MHz	1600 LUT6s
Virtex-7	Host	1,500 Mbit/s	187 MHz	1200 LUT6s
	Peripheral	1,500 Mbit/s	187 MHz	1600 LUT6s
Zynq-7000 Kintex-7	Host	1,500 Mbit/s	187 MHz	1200 LUT6s
	Peripheral	1,500 Mbit/s	187 MHz	1600 LUT6s
Zynq-7000 Artix-7	Host	1,250 Mbit/s	156 MHz	1200 LUT6s
	Peripheral	1,250 Mbit/s	156 MHz	1600 LUT6s
Spartan-6	Host	1,080 Mbit/s	135 MHz	1200 LUT6s
	Peripheral	1,080 Mbit/s	135 MHz	1600 LUT6s

Notes:

1. Assumes the use of the HP I/O. Contact Rambus for supported HR I/O rates
2. Zynq-7000 devices are either Kintex-7 or Artix-7 fabric based
3. Data Rate limited to 1,500 Mbit/s per MIPI specification even if device supports faster LVDS rates
4. Clock Rate 1/8th of Data Rate
5. 4 D-PHY lane implementation
6. Support of LogiCORE D-PHY data rates up to 2,500 Mbit/s per lane available with Kintex Ultrascale+ or Zynq Ultrascale+