Rambus

PCI Express IP Core Size & Speed
FPGA

To The Point Solutions

Version 4.65

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Introduction

Rambus provides a broad range of high-performance, easy-to-use IP Cores. This document summarizes the speed and size for each of these cores for a variety of devices. It is important to note that the speed and size are "typical maximum" values. The actual speed and size is dependent on a wide variety of factors including:

- Device speed grade
- Core configuration (data width, etc.)

Contact Rambus to review your overall design requirements and receive a more specific core speed and size for your target device and design requirements.

For more information on Rambus and our IP Cores:

- Visit our website at www.rambus.com
- Send an e-mail to rcg@rambus.com

AXI DMA Back-End Core and DMA Back-End Core

Device	PCI Express Core	x1		x2		x4		x8		
		32 bit	64 bit	32 bit	64 bit	64 bit	128 bit	64 bit	128 bit	256 bit
Stratix 10	Intel PSG Hard IP Block		6,240 ALUTs 6 M20K RAMs		6,240 ALUTs 6 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	23,000 ALUTs 8 M20K RAMs
Stratix V	Intel PSG Hard IP Block		6,240 ALUTs 6 M20K RAMs		6,240 ALUTs 6 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	23,000 ALUTs 8 M20K RAMs
Stratix IV	Intel PSG Hard IP Block		6,240 ALUTs 6 M9K RAMs		6,240 ALUTs 6 M9K RAMs	7,600 ALUTs 6 M9K RAMs	9,075 ALUTs 8 M9K RAMs	7,600 ALUTs 6 M9K RAMs	9,075 ALUTs 8 M9K RAMs	
Arria 10	Intel PSG Hard IP Block		6,240 ALUTs 6 M20K RAMs		6,240 ALUTs 6 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	23,000 ALUTs 8 M20K RAMs
Arria V GZ	Intel PSG Hard IP Block		6,240 ALUTs 6 M20K RAMs		6,240 ALUTs 6 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	7,600 ALUTs 6 M20K RAMs	9,075 ALUTs 8 M20K RAMs	23,000 ALUTs 8 M20K RAMs
Arria V	Intel PSG Hard IP Block		8,000 ALUTs 6 M10K RAMs			10,500 ALUTs 6 M10K RAMs	13,000 ALUTs 8 M10K RAMs	10,500 ALUTs 6 M10K RAMs	13,000 ALUTs 8 M10K RAMs	
Cyclone V	Intel PSG Hard IP Block		8,000 ALUTs 6 M10K RAMs			10,500 ALUTs 6 M10K RAMs				

Notes:

1. AXI Interface utilizes additional 6,130 ALUTs, 20 M20K/M9K RAMs

2. This utilization is based on 1 S2C and 1 C2S engines with 64 bit address support, reorder queue with 4 (x1, x2 lanes), 8 (x4, x8 lanes), 16 (x8 lane, 256 bit) completion tags. See below for the completion tags used in each configuration that could be utilized for maximum perfomance:

	x1		x2		x4		x8		
	32 bit	64 bit	32 bit	64 bit	64 bit	128 bit	64 bit	128 bit	256 bit
PCIe Gen 1.1	4	4	4	4	8	8	8	8	
PCIe Gen 2.1	4	4	4	4	8	8	16	16	
Pcie Gen 3.0	4	4	8	8	16	16		16	16

Contact Rambus for the size of other configurations.

DMA Back-End Core

Device	PCI Express Core	x1		x2	x2/x4	x4	x8			x16
		32 bit	64 bit	32 bit	64 bit	128 bit	64 bit	128 bit	256 bit	512 bit
Virtex UltraScale+ Kintex UltraScale+ Zynq UltraScale+	Xilinx Hard IP Block		8,500 LUT6s 6 36K RAMs		8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	22,000 LUT6s 12 36K RAMs	57,000 LUT6s 24 36K RAMs
Virtex UltraScale Kintex UltraScale Zynq UltraScale	Xilinx Hard IP Block		8,500 LUT6s 6 36K RAMs		8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	22,000 LUT6s 12 36K RAMs	
Zynq-7000 Virtex-7 Kintex-7 Artix-7	Xilinx Hard IP Block		8,500 LUT6s 6 36K RAMs		8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	8,500 LUT6s 6 36K RAMs	9,550 LUT6s 8 36K RAMs	22,000 LUT6s 12 36K RAMs	

Notes:

1. This utilization is based on 1 S2C and 1 C2S engines with 64 bit address support, reorder queue with 4 (x1, x2 lanes), 8 (x4, x8 lanes), 16 (x8, 256 bit), 16 (x16, 512 bit) completion tags. See below for the completion tags used in each configuration that could be utilized for maximum perfomance:

	x1		x2		x4		x8			x16
	32 bit	64 bit	32 bit	64 bit	64 bit	128 bit	64 bit	128 bit	256 bit	512 bit
PCIe Gen 1.1	4	4	4	4	8	8	8	8		
PCIe Gen 2.1	4	4	4	4	8	8	16	16		
Pcie Gen 3.0	4	4	8	8	16	16		16	16	16

	x1	x2	x4	x8
	64 bit	128 bit	256 bit	512 bit
Pcie Gen 4.0	8	16	16	16

Contact Rambus for the size of other configurations.

AXI DMA Back-End Core

Device	PCI Express Core	x1		x2	x2/x4	x4	x8		
		32 bit	64 bit	32 bit	64 bit	128 bit	64 bit	128 bit	256 bit
Virtex UltraScale+ Kintex UltraScale+ Zynq UltraScale+	Xilinx Hard IP Block		11,000 LUT6s 10 36K RAMs		11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	37,000 LUT6s 33 36K RAMs
Virtex UltraScale Kintex UltraScale Zynq UltraScale	Xilinx Hard IP Block		11,000 LUT6s 10 36K RAMs		11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	37,000 LUT6s 33 36K RAMs
Zynq-7000 Virtex-7 Kintex-7 Artix-7	Xilinx Hard IP Block		11,000 LUT6s 10 36K RAMs		11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	11,000 LUT6s 10 36K RAMs	21,000 LUT6s 13 36K RAMs	37,000 LUT6s 33 36K RAMs

Notes:

1. This utilization is based on 1 S2C and 1 C2S engines with 64 bit address support, reorder queue with 4 (x1, x2 lanes), 8 (x4, x8 lanes), 16 (x8, 256 bit) completion tags. See below for the completion tags used in each configuration that could be utilized for maximum perfomance:

	x1		x2		x4		x8		
	32 bit	64 bit	32 bit	64 bit	64 bit	128 bit	64 bit	128 bit	256 bit
PCIe Gen 1.1	4	4	4	4	8	8	8	8	
PCIe Gen 2.1	4	4	4	4	8	8	16	16	
Pcie Gen 3.0	4	4	8	8	16	16		16	16

	x1	x2	x4	x8
	64 bit	128 bit	256 bit	512 bit
Pcie Gen 4.0	8	16	16	16

Contact Rambus for the size of other configurations.