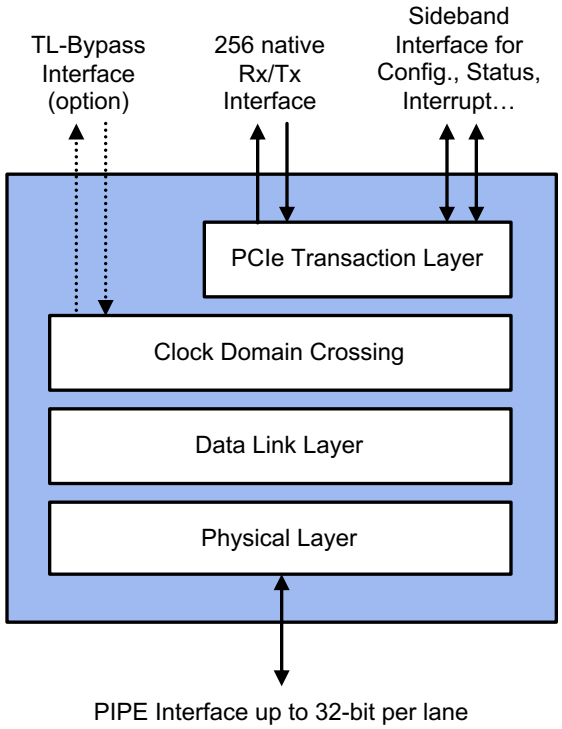
PCI Express 4.0 Controller

Optimized for high-bandwidth efficiency to deliver maximum performance for Data Center, Edge, AI/ML and HPC applications.

Overview

The Rambus PCI Express® (PCIe) 4.0 Controller is a configurable and scalable design for ASIC and FPGA implementations. It is backward compatible to PCIe 3.1/3.0, and supports version 4.x PHY Interface for PCI Express (PIPE) specification. When combined with the Rambus PCIe 4.0 PHY, it comprises a complete PCIe 4.0 interface subsystem.

PCIe 4.0 Controller Block Diagram



Highlights

- Comprises a complete PCIe 4.0 interface subsystem with the Rambus PCIe 4.0 PHY
- Supports Root Port, Endpoint, Dual-Mode and Switch Port
- Automatically scalable 64 to 256-bit data path
- Superior Transmit and Receive latency
- Smart buffer management on receive side (Rx Stream) and transmit side (merged Replay/Transmit buffer) enables lower memory footprint
- Dynamically adjustable application layer frequency down to 8 Mhz for increased power savings
- Allows seamless migration from FPGA prototyping to ASIC/SoC production
- Supports advanced RAS features

Protocol Compatibility

Protocol	**Data Rates** (GT/s)
PCIe 3.1/3.0	8
PCIe 4.0	16

How It Works

The PCIe 4.0 Controller can be configured to support endpoint, root port, switch port, and dual-mode topologies, allowing for a variety of use models. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters.

Its flexible architecture supports a variety of use cases, tailored to unique customer needs. The PCIe 4.0 Controller builds on a family of PCIe controller designs that have been deployed in over 400 tape-outs since the PCIe 1.1 generation of the standard.

Features

PCI Express Layer

- Compliant with the PCI Express 4.0 (16 GT/s), 3.1/3.0 (8 GT/s), and PIPE 4.x (8-, 16- and 32-bit) specifications
- Compliant with PCI-SIG Single-Root I/O Virtualization (SR-IOV) Specification
- Supports Endpoint, Root-Port, Dual-mode configurations
- Supports x16, x8, x4, x2, x1 at Gen4, Gen3, Gen2, Gen1 speeds
- Supports RAS, AER, ECRC, ECC, MSI, MSI-X, Multifunction, crosslink, and other optional features
- Additional optional features include OBFF, TPH, ARI, LTR, IDO, L1 PM substates, etc.
- Supports FPGA platforms up to PCIe 4.0 x8

User Interface Layer

- 256-bit transmit/receive low-latency user interface
- User-selectable Transaction/Application Layer clock frequency
- Sideband signaling for PCIe configuration access, internal status monitoring, debug, and more
- Optional Transaction Layer bypasss

Deliverables

IP Files

- Verilog RTL source code
- Libraries for functional simulation
- Configuration assistant GUI (Wizard)
- Testbench in source code

Documentation

Software

- PCI Express Windows and Linux device drivers
- Optional: source code drivers
- C API
- Reference design test executable and C++/Java source code

PCI Express Bus Functional Model

- Simulation libraries
- Support from expert application engineers and IP designers
- Testbench in source code

rambus.com/pci-express-controllers