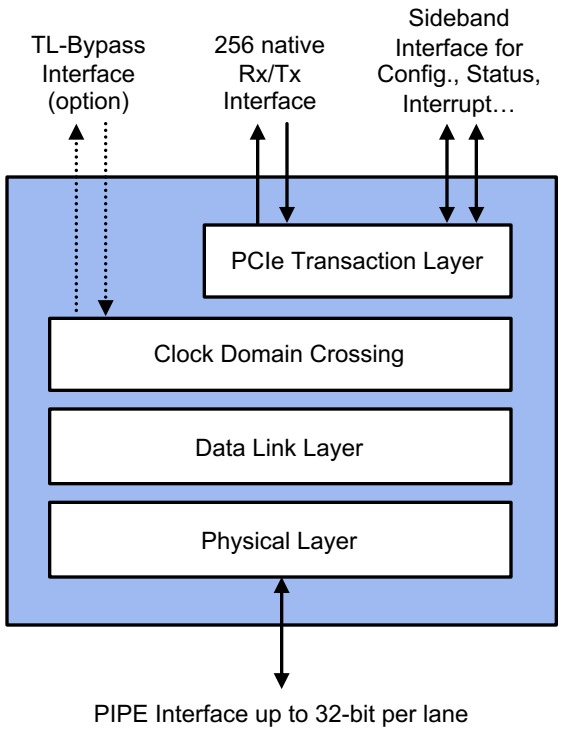
PCI Express 3.1 Controller

Optimized for high-bandwidth efficiency to deliver maximum performance for Data Center, Edge, AI/ML and HPC applications.

Overview

The Rambus PCI Express® (PCIe) 3.1 Controller is designed to achieve maximum PCIe 3.1 performance with great design flexibility and ease of integration. It is fully compatible with the PCIe 3.1/3.0 specification. The controller delivers high-bandwidth and low-latency connectivity for demanding applications in data center, edge and graphics.

PCIe 3.1 Controller Block Diagram



Highlights

- Supports Root Port, Endpoint, Switch Port, and Dual-Mode topologies
- Advanced features enable fine tuning of power, area, throughput and latency
- Internal data path size automatically scales up or down based on link max. speed and width
- Optional QuickBoot mode allows for up to 4x faster link training
- Supports advanced RAS features

Protocol Compatibility

Protocol	Data Rates (GT/s)
PCIe 2.1/1.0	5
PCIe 3.1/3.0	8

How It Works

The PCIe 3.1 Controller is configurable and scalable IP designed for ASIC and FPGA implementation. It supports the PCIe 3.1/3.0 specifications, as well as the PHY Interface for PCI Express (PIPE) specification. The IP can be configured to support endpoint, root port, switch port, and dual-mode topologies, allowing for a variety of use models. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters, including data path size, PIPE interface width, low power support, SR-IOV, ECC, AER, etc. for optimal throughput, latency, size and power. The PCIe 3.1 Controller is verified using multiple PCIe VIPs and test suites, and is silicon proven in hundreds of designs in production.

PCI Express Layer

- Compliant with the PCI Express 3.1/3.0, and PIPE (16- and 32-bit) specifications
- Compliant with PCI-SIG Single-Root I/O Virtualization (SR-IOV) Specification
- Supports Endpoint, Root-Port, Dual-mode, Switch port configurations
- Supports x16, x8, x4, x2, x1 at 8 GT/s, 5 GT/s, 2.5 GT/s speeds
- Supports RAS, AER, ECRC, ECC, MSI, MSI-X, Multi-function, crosslink, and other optional features
- Additional optional features include OBFF, TPH, ARI, LTR, IDO, L1 PM substates, etc.

User Interface Layer

- 256-bit transmit/receive low-latency user interface
- User-selectable Transaction/Application Layer clock frequency
- Sideband signaling for PCIe configuration access, internal status monitoring, debug, and more
- Optional Transaction Layer bypass

Unique Features & Capabilities

- Dynamically adjustable application layer frequency down to 8Mhz for increased power savings
- Optional MSI/MSI-X register remapping to memory for reduced gate count when SR-IOV is implemented
- Configurable pipelining enables full speed operation on Intel and Xilinx FPGA, full support for production FPGA designs up to Gen3 x16 with same RTL code
- Ultra-low Transmit and Receive latency
- Smart buffer management on receive side (Rx Stream) and transmit side (merged Replay/Transmit buffer) enables lower memory footprint
- Optional Transaction Layer bypass allows for customer specific transaction layer and application layer
- Optional QuickBoot mode allows for up to 4x faster link training, cutting system-level simulation time by 20%

Deliverables

IP Files

- Verilog RTL source code
- Libraries for functional simulation
- Configuration assistant GUI

Documentation

PCI Express Bus Function Model

- Encrypted Simulation libraries

Software

- PCI Express Windows x64 and Linux x64 device drivers
- PCIe C API

Reference Designs

- Synthesizable Verilog RTL source code
- Simulation environment and test scripts
- Synthesis project & DC constraint files (ASIC)
- Synthesis project & constraint files for supported FPGA hardware platforms (FPGA)

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