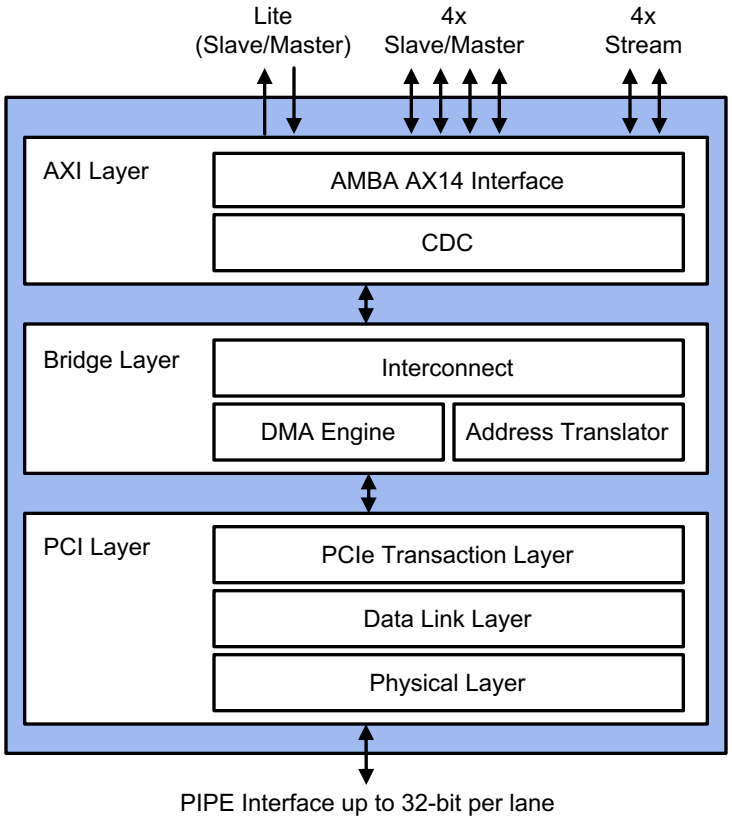
PCI Express 3.1 Controller with AXI

Optimized for high-bandwidth efficiency to deliver maximum performance for Data Center, Edge, AI/ML and HPC applications.

Overview

The Rambus PCI Express® (PCIe) 3.1 Controller with AXI is a configurable and scalable PCIe controller Soft IP designed for ASIC and FPGA implementation. It supports the PCI Express 3.1/3.0 specifications, as well as the PHY Interface for PCI Express (PIPE) specification and the AMBA® AXI™ Protocol Specification.

PCIe 3.1 Controller with AXI Block Diagram



Highlights

- Supports Root Port, Endpoint, and Dual-Mode topologies
- Advanced features enable fine tuning of power, area, throughput and latency
- PCIe to AXI and AXI to PCIe Ordering Rules guarantee AXI deadlock prevention
- AXI bridge & AXI interconnect allows full performance on AXI interfaces
- Internal data path size automatically scales up or down based on link max. speed and width
- Optional QuickBoot mode allows for up to 4x faster link training
- Supports advanced RAS features

Protocol Compatibility

Protocol	Data Rates (GT/s)
PCIe 2.1/2.0	5
PCIe 3.1/3.0	8

How It Works

The PCIe 3.1 Controller is configurable and scalable IP designed for ASIC and FPGA implementation. It supports the PCIe 3.1/3.0 specifications, as well as the PHY Interface for PCI Express (PIPE) specification. The IP can be configured to support endpoint, root port, and dual-mode topologies, allowing for a variety of use models. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters, including data path size, PIPE interface width, low power support, SR-IOV, ECC, AER, etc. for optimal throughput, latency, size and power. The PCIe 3.1 Controller is verified using multiple PCIe VIPs and test suites, and is silicon proven in hundreds of designs in production.

PCI Express Layer

- Compliant with the PCI Express 3.1/3.0, and PIPE (16- and 32-bit) specifications
- Compliant with PCI-SIG Single-Root I/O Virtualization (SR-IOV) Specification
- Supports Endpoint, Root-Port, Dual-mode configurations
- Supports x16, x8, x4, x2, x1 at 8 GT/s, 5 GT/s, 2.5 GT/s speeds
- Supports RAS, AER, ECRC, ECC, MSI, MSI-X, Multi-function, P2P, crosslink, and other optional features
- Supports many ECNs including LTR, L1 PM substates, etc.

AMBA AXI Layer

- Compliant with the AMBA® AXI™ Protocol Specification (AXI3, AXI4 and AXI4-Lite) and AMBA® 4 AXI4-Stream Protocol Specification
- Supports multiple, user-selectable AXI interfaces including AXI Master, AXI Slave, AXI Stream
- Each AXI interface data width independently configurable in 512-, 256-, 128-, and 64-bit
- Each AXI interface can operate in a separate clock domain

Data Engines

- Built-in legacy DMA engine:
  - Up to 8 DMA channels, Scatter-Gather, descriptor prefetch
  - Completion reordering, interrupt and descriptor reporting
- Optional Address Translation tables for direct PCIe to AXI and AXI to PCIe communication

Deliverables

IP Files

- Verilog RTL source code
- Libraries for functional simulation
- Configuration assistant GUI

Documentation

PCI Express Bus Function Model

- Encrypted Simulation libraries

Software

- PCI Express Windows x64 and Linux x64 device drivers
- PCIe C API

Reference Designs

- Synthesizable Verilog RTL source code
- Simulation environment and test scripts
- Synthesis project & DC constraint files (ASIC)
- Synthesis project & constraint files for supported FPGA hardware platforms (FPGA)

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