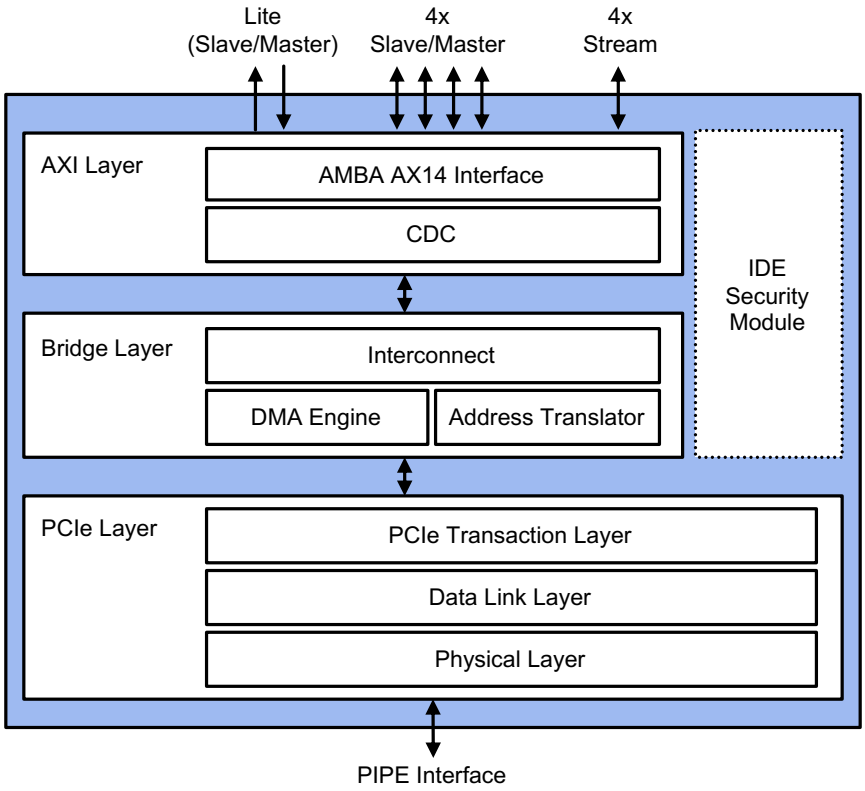
PCI Express 5.0 Controller with AXI

Optimized for high-bandwidth efficiency to deliver maximum performance for Data Center, Edge, AI/ML and HPC applications.

Overview

The Rambus PCI Express® (PCIe) 5.0 Controller with AXI is a configurable and scalable design for ASIC and FPGA implementations. It is backward compatible to PCIe 4.0 and 3.1/3.0, and compatible with version 5.x of PHY Interface for PCI Express (PIPE) specification and the AMBA® AXI™ Protocol Specification.

PCIe 5.0 Controller with AXI Block Diagram



Highlights

- Supports Root Port, Endpoint and Dual-Mode
- Advanced features enable fine tuning of power, area, throughput and latency
- PCIe to AXI and AXI to PCIe Ordering Rules guarantee AXI deadlock prevention
- AXI bridge & AXI interconnect allows full performance on AXI interfaces
- Internal data path size automatically scales up or down based on link max. speed and width
- Each AMBA AXI user interface can be configured independently from 64-bit to 512-bit and with independent clock speeds to provide a variety of connectivity options
- QuickBoot mode allows for up to 4x faster link training
- Supports advanced RAS features

Protocol Compatibility

Protocol	**Data Rates** (GT/s)
PCIe 3.1/3.0	8
PCIe 4.0	16
PCIe 5.0	32

How It Works

The PCIe 5.0 Controller with AXI can be configured to support endpoint, root port, and dual-mode topologies, allowing for a variety of use models, and exposes a configurable, flexible AMBA AXI interconnect interface to the user. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters.

Users may optionally enable the built-in legacy DMA engine, or connect a DMA engine externally depending on the application requirements. Rambus provides integration and validation of the PCIe 5.0 digital controller with the customer's choice of 3rd-party PCIe 5.0 PHY.

Features

PCI Express Layer

- Compliant with the PCI Express 5.0 rev 1.0 (32GT/s), 4.0 (16 GT/s), 3.1/3.0 (8 GT/s), and PIPE 5.x (8-, 16-, 32-, and 64-bit) specifications
- Supports PCI-SIG Single-Root I/O Virtualization (SR-IOV) specification
- Supports Endpoint, Root-Port, Dual-mode configurations
- Supports x16, x8, x4, x2, x1 at 16 GT/s, 8 GT/s, 5 GT/s, 2.5 GT/s speeds
- Supports RAS, AER, ECRC, ECC, MSI, MSI-X, Multi-function, P2P, crosslink, and other optional features
- Supports many ECNs including LTR, L1 PM substates, etc.

AMBA AXI Layer

- Compliant with the AMBA AXI Protocol specification (AXI3, AXI4 and AXI4-Lite) and AMBA 4 AXI4-Stream Protocol specification
- Supports multiple, user-selectable AXI interfaces, including AXI Master, AXI Slave, AXI Stream
- Each AXI interface data width independently configurable as 512-, 256-, 128-, and 64-bit
- Each AXI interface can operate in a separate clock domain

Integrity and Data Encryption (IDE)

- Implements the PCI Express IDE ECN
- Configurable IDE engine
  - Supports x1 to x16 lanes
  - 256-bit or 512-bit data bus for PCIe IDE
- Supports containment and skid modes
- Supports early MAC termination
- Supports multi-stream
- Utilizes high-performance AES-GCM for encryption, decryption, authentication
- PCIe IDE TLP aggregation for 1, 2, 4, 8 TLPs
- PCIe IDE automatic IDE prefix insertion and detection
- PCIe IDE automatic IDE sync/fail message generation
- PCRC calculation & validation
- Efficient key control/refresh
- Bypass mode

Data Engines

- Built-in legacy DMA engine:
  - Up to 8 DMA channels, Scatter-Gather, descriptor prefetch
  - Completion reordering, interrupt and descriptor reporting
- Optional Address Translation tables for direct PCIe to AXI and AXI to PCIe communication

Deliverables

IP Files

- Verilog RTL source code
- Libraries for functional simulation
- Configuration assistant GUI (Wizard)
- PCI Express Bus Functional Model
- Encrypted simulation libraries

Documentation

Software

- PCI Express Windows x64 and Linux x64 device drivers
- PCIe C API

Reference Designs

- Synthesizable Verilog RTL source code
- Simulation environment and test scripts
- Synthesis project and DC constraint files (ASIC)
- Synthesis project and constraint files for supported FPGA hardware platforms (FPGA)

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