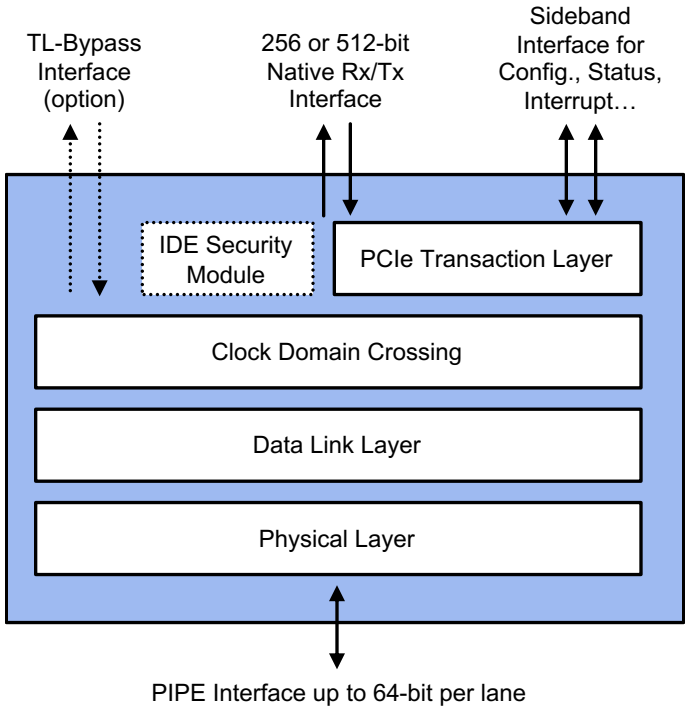
PCI Express 5.0 Controller

Optimized for high-bandwidth efficiency to deliver maximum performance for Data Center, Edge, AI/ML and HPC applications.

Overview

The Rambus PCI Express® (PCIe) 5.0 Controller is a configurable and scalable design for ASIC and FPGA implementations. It is backward compatible to PCIe 4.0 and 3.1/3.0, and supports version 5.x PHY Interface for PCI Express (PIPE) specification.

PCIe 5.0 Controller Block Diagram



Highlights

- Supports Root Port, Endpoint, Dual-Mode and Switch Port
- Automatically scalable 256/512-bit data path
- Superior Transmit and Receive latency
- Smart buffer management on receive side (Rx Stream) and transmit side (merged Replay/Transmit buffer) enables lower memory footprint
- Optional Transaction Layer bypass allows for customer specific transaction layer and application layer
- QuickBoot mode allows for up to 4x faster link training, cutting system-level simulation time by 20%
- Configurable pipelining enables full speed operation on leading FPGAs
- Allows seamless migration from FPGA prototyping to ASIC/SoC production
- Supports advanced RAS features

Protocol Compatibility

Protocol	**Data Rates** (GT/s)
PCIe 3.1/3.0	8
PCIe 4.0	16
PCIe 5.0	32

How It Works

The PCIe 5.0 Controller can be configured to support endpoint, root port, switch port, and dual-mode topologies, allowing for a variety of use models. The provided Graphical User Interface (GUI) Wizard allows designers to tailor the IP to their exact requirements, by enabling, disabling, and adjusting a vast array of parameters.

Its flexible architecture supports a variety of use cases, tailored to unique customer needs. Rambus provides integration and validation of the PCIe 5.0 digital controller with the customer's choice of 3rd-party PCIe 5.0 PHY.

Features

PCI Express Layer

- Compliant with the PCI Express 5.0 rev 1.0 (32GT/s), 4.0 (16 GT/s), 3.1/3.0 (8 GT/s), and PIPE 5.x (8-, 16-, 32-, and 64-bit) specifications
- Compliant with PCI-SIG Single-Root I/O Virtualization (SR-IOV) Specification
- Supports Endpoint, Root-Port, Dual-mode, Switch port configurations
- Supports x16, x8, x4, x2, x1 at Gen5, Gen4, Gen3, Gen2, Gen1 speeds
- Supports AER, ECRC, ECC, MSI, MSI-X, Multifunction, crosslink, and other optional features
- Additional optional features include OBFF, TPH, ARI, LTR, IDO, L1 PM substates, etc.
- RAS features include LTSSM timers override, ACK/NAK/Replay/UpdateFC timers override, unscrambled PIPE interface access, error injection on Rx and Tx paths, recovery detailed status and much more, allowing for safe and reliable deployment of IP in mission-critical SoCs

User Interface Layer

- 512-bit or 256-bit transmit/receive low-latency user interface
- Up to 2 TLP per clock cycle (TLP chaining)
- User-selectable Transaction/Application Layer clock frequency
- Sideband signaling for PCIe configuration access, internal status monitoring, debug, and more
- Optional Transaction Layer bypasss

Integrity and Data Encryption (IDE) – Optional

- Implements the PCI Express IDE ECN
- Configurable IDE engine
  - Supports x1 to x16 lanes
  - 256-bit or 512-bit data bus for PCIe IDE
- Supports containment and skid modes
- Supports early MAC termination
- Supports multi-stream
- Utilizes high-performance AES-GCM for encryption, decryption, authentication
- PCIe IDE TLP aggregation for 1, 2, 4, 8 TLPs
- PCIe IDE automatic IDE prefix insertion and detection
- PCIe IDE automatic IDE sync/fail message generation
- PCRC calculation & validation
- Efficient key control/refresh
- Bypass mode

Deliverables

IP Files

- Verilog RTL source code
- Libraries for functional simulation
- Configuration assistant GUI (Wizard)
- PCI Express Bus Functional Model
- Encrypted simulation libraries

Documentation

Software

- PCI Express Windows x64 and Linux x64 device drivers
- PCIe C API

Reference Designs

- Synthesizable Verilog RTL source code
- Simulation environment and test scripts
- Synthesis project and DC constraint files (ASIC)
- Synthesis project and constraint files for supported FPGA hardware platforms (FPGA)

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