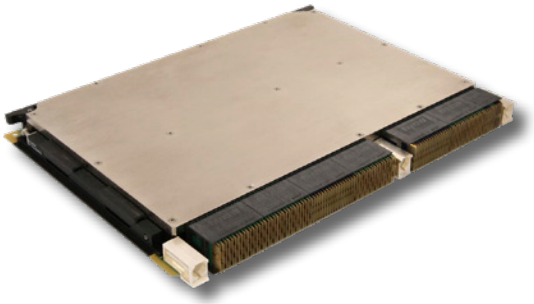
CHAMP-XD2M

High Memory Capacity Multi-Core HPEC Module based on the Intel Xeon Processor D

CURTISS-WRIGHT

CURTISSWRIGHTDS.COM



Key Features

- Xeon D 16-core processor (870 GFLOPS @ 1.7 GHz)
- Alternative Xeon D SKUs available
- 128 GB DDR4 @ 2133 MT/s (34 GBps over 2 ECC channels)
- Four ports of 40G/10G Ethernet or DDR/QDR/FDR10 InfiniBand on OpenVPX data plane
- Native dual KX 1 GigE or KR 10 GigE ports on OpenVPX control plane
- XMC PCIe up to Gen3, designed for up to 25W thermal dissipation
- Dual x16 PCIe Gen3 on OpenVPX expansion plane with switch
- PCH integrated in Xeon D SoC
- Core Function FPGA (Xilinx UltraScale) and IPMI (Microsemi SmartFusion)
- Air and conduction-cooled
- TrustedCOTS

Applications

- Sensor fusion
- Mobile platform server
- Synthetic Aperture Radar (SAR)
- Signal Intelligence (SIGINT)
- Electro-Optical/Infrared (EO/IR)
- Mission computing
- Industrial server applications

Overview

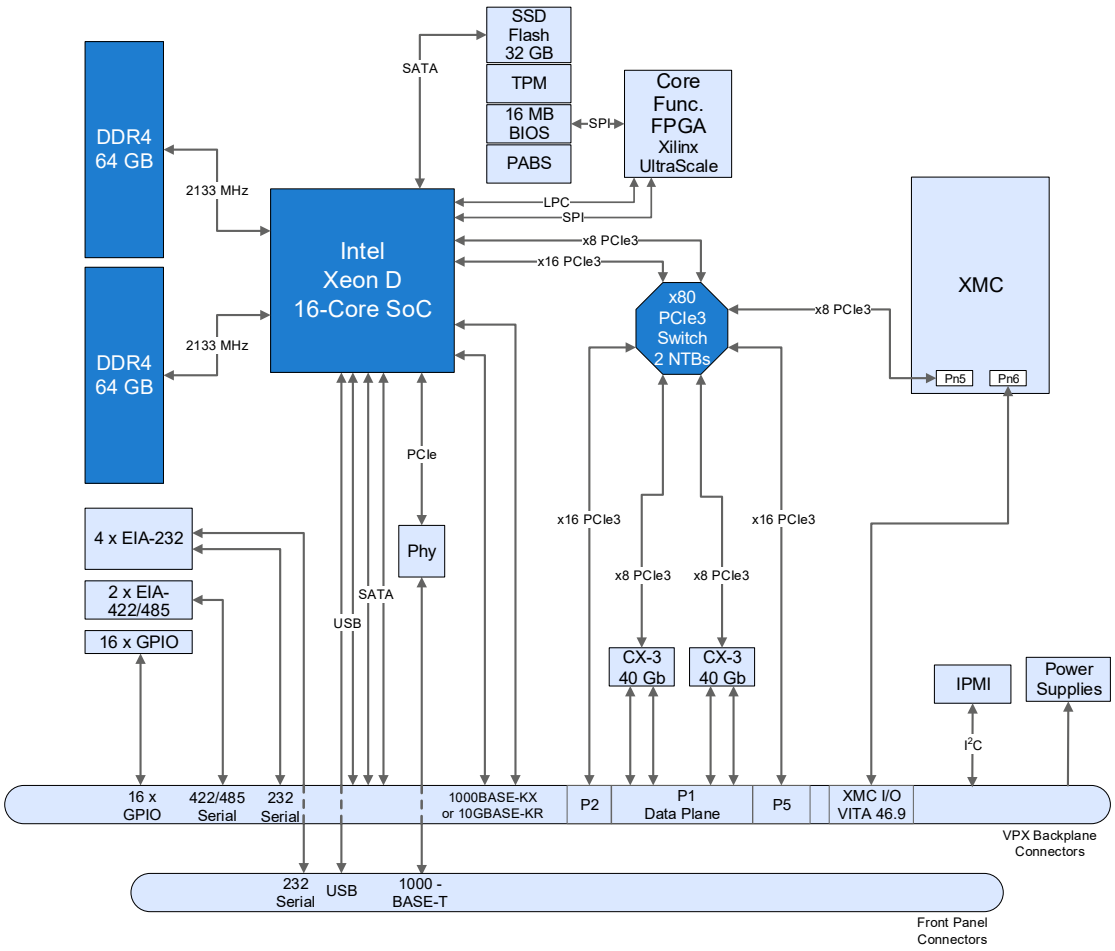
The 6U OpenVPX™ CHAMP-XD2M rugged Intel® Xeon® D module is designed for use in high memory capacity, compute-intensive Industrial, Aerospace and Defense applications, enabling developers of High Performance Embedded Computing (HPEC) systems to take full advantage of the unmatched performance of today's leading-edge Xeon processor D architecture.

The CHAMP-XD2M combines the high core count and floating-point performance of the Xeon D processor with a massive 128 GB (maximum capacity supported by Xeon D) in addition to the substantial bandwidth and system-enabling features of the VITA 6U OpenVPX form factor. Providing a 16 core Intel Xeon D processor, the CHAMP-XD2M has a peak performance of 870 GFLOPS. This is coupled with 128 GB of high capacity DDR4-2133, with a bandwidth of >17 GBps per channel, two channels total of ECC memory.

For high speed data transport, the CHAMP-XD2M supports 40 G / 10 G Ethernet or InfiniBand® on the data plane in addition to 1 Gigabit (Gb) or 10 Gigabit Ethernet (GbE) interfaces along the OpenVPX control plane. The CHAMP-XD2M's XMC mezzanine site (designed for up to 25W of thermal dissipation) adds even more configuration flexibility, with a myriad of mezzanine cards available from both Curtiss-Wright and other industry vendors.

The CHAMP-XD2M is available in a range of ruggedized configurations to deliver optimal performance in the harshest deployed environments, including air-cooled and conduction-cooled variants. There is also resident a Core Function field programmable gate array (Xilinx® UltraScale™ FPGA) used for TrustedCOTS™ security and general purpose I/O in addition to a dedicated Intelligent Platform Management Interface (IPMI) FPGA used for system monitoring and health.

Leveraging Curtiss-Wright's extensive 6U OpenVPX ecosystem, the CHAMP-XD2M forms the centerpiece of high memory capacity, high core count HPEC system architectures. Other Curtiss-Wright 6U OpenVPX modules available for HPEC configurations include the dual Xeon D based CHAMP-XD2, VPX6-1958/VPX6-1959 Single Board Computers, VPX6-6802 Ethernet/InfiniBand Switch, CHAMP-GP GPGPU Processors, and CHAMP-FX4 FPGA-based ADC/DAC modules.



CHAMP-XD2M block diagram

Specifications

Xeon D 16 Core Processor

- Intel Xeon D (D-1587) 16 Core 1.7 GHz Processor (870 GFLOPS) with integrated Platform Controller Hub (PCH)
- Alternate extended temp SKUs available such as 8 and 12 cores (410 to 576 GFLOPS)
- Up to 65W TDP packages supported
- 14 nm process technology
- 1.5 MB max last level cache per core
- 2-channel DDR4 memory controller with transfer rates up to 2133 MT/s
- 16-lane and 8-lane PCI Express® (PCIe) Gen3 interfaces from processor to PCIe switch
- Serial ATA (SATA 3.0) controller – 2 ports, 6 Gbps support
- Low Pin Count (LPC) Interface between processor and Core Function FPGA
- 2 x USB EHCI host controllers – up to 2 ports, USB 2.0/ USB 3.0
- Serial Peripheral Interface (SPI) – up to 50 MHz
- SMBus 2.0 up to 100 Kbps
- Enhanced DMA controller
- Integrated GbE LAN controller
- 2 x 10G Ethernet interfaces
- JTAG 1149.1

Volatile memory per processor

- 2 x channels DDR4 SDRAM, 2133 MTps, 34 GBps total (17 GBps per channel)
- 128 GB total (64 GB per channel)
- ECC

Non-volatile memory

- SSD – SATA Gen2, NAND Flash, 32 GB
- SPI Flash for BIOS (16 MB), x 2 including PABS, per processor node
- NVRAM (512 KBytes)

On-board interconnects

- LPC, PCH to Core FPGA
- SPI, PCH to Core FPGA
- TPM, BIOS and PABS route through Core FPGA
- PCH SMBus 2.0/I2C to PCIe switch for field update
- IPMC FPGA to SMLink (SMBus) interface of PCH for temperature data
- SATA Gen3 to backplane, two ports
- PCIe Gen3, processor to PCIe switch, one x16 connection and one x8 connection
- PCIe Gen2, PCH to i210 Ethernet NIC and Core FPGA
- PCIe Gen3, 2 x ConnectX3 devices to PCIe switch

Mezzanine site

- 1 x XMC with PCIe Gen2/Gen3 with connection to PCIe switch
  - VITA 46.9 X38s+X8d+X12d

Peripherals

- 10 GbE
  - 2 x 10GBASE-KR / 1000BASE-KX
- GbE
  - 1 x 10/100/1000BASE-T on front panel (air-cooled only) or backplane (air-cooled and conduction-cooled)
- PCIe
  - 80-lane, 20-port switch
  - 1 x 16 PCIe Gen3 port from processor to switch
  - 1 x 8 PCIe Gen3 port from processor to switch
  - 1 x 8 non-transparent port on processor
  - 2 NTB ports supported on PCIe switch
  - x16 from Switch to VPX P2
  - x16 from Switch to VPX P5
  - One x8 from Switch to XMC
- SATA 2.0
  - Solid Disk Drive Flash
- SATA 3.0
  - 2 x to backplane
- USB 2.0
  - 1 x USB 2.0 ports to the front panel or backplane
- USB 3.0
  - 1 x USB 3.0 ports to the backplane
- Digital I/O (DIO)
  - Up to 8 x interrupt-capable DIO
  - Up to 2 x differential I/O
- Serial ports
  - 2 x RS-232 connected to both the front panel and backplane
  - 2 x RS-422/485

Test headers

- JTAG – available on RTM for programming

I2C/SMBus devices

- Temperature and voltage sense integrated into IPMI solution

Core Function FPGA (Xilinx UltraScale KU035)

- Provides logical hardware services for CHAMP-XD2M
- Interfaces to Intel Xeon D Processor through LPC bus
- Uses Curtiss-Wright common hardware reuse blocks
- Interrupt controller supports serial IRQ protocol
- 4 x 16550-compatible UART serial ports (2 x RS-232 and 2 x RS-422/485)
- 1 x internal dedicated 16550-compatible UART serial port (for IPMC comm)
- 1 x watchdog timer
- 6 x general-purpose timers
- Port 80 registers
- Internal low-latency, high-performance bus switch between processor complex and target
- SPI interface to external TPM/main Flash/PABS
- SPI interface to external NVRAM (accessed through LPC)
- Multi-Board Synchronous Counter (MBSC) using backplane sync/clock signals
- Board configuration/status registers
- Jumper status registers
- 8 channels of Discrete LVTTL I/O (DIO) and 2 channels of Differential Discrete RS-422 I/O (DDIO)
- JTAG I/O port for IPMI FPGA configuration programming
- Reset control (in conjunction with reset CPLD)
- Reset cause registers
- 16 x semaphore registers

IPMC FPGA (MicroSemi SmartFusion)

- Proven FPGA fabric
- Complete ARM® Cortex™-M3 MCU subsystem
- Flash-based device
- 2 x status LED outputs
- 1 x fail LED output
- XMC status registers
- VPX geographical address status registers
- Field Upgradable Unit (FRU) information storage
- 4 x voltage and 4 x temperature sensors (programmable ADCs)
- UART interface to Core FPGA

Trusted Platform Module (TPM)

- SPI based Atmel AT97SC3205

Mechanical

- Air-cooled L0/L100
- Conduction-cooled L100/L200

Power

- Standard product: Consult Curtiss-Wright

Software

- Operating system support: Red Hat® Enterprise Linux®
- Additional OS and RTOS support including Wind River® VxWorks® 7.0: contact Curtiss-Wright for more information
- Communications support via MPI/OFED

Unparalleled PCI Express Flexibility

The CHAMP-XD2M incorporates a PEX 8780 80 lane/20 port PCIe Gen3 Switch, which contains two Non-Transparent Bridges (NTBs) essential for complex PCIe system-wide interconnect. A total of 24 PCIe lanes from the Xeon D, 32 lanes from the OpenVPX expansion plane,16 lanes from the Ethernet/InfiniBand based data plane, and 8 lanes from the XMC mezzanine all aggregate to the switch. A wide array of partitioning schemes is possible with the Broadcom PEX 8780 Switch providing developers with excellent flexibility in system design.

Superior XMC Mezzanine Support

Considerable attention has been applied to the XMC site on the CHAMP-XD2M, which has been thermally designed to handle substantial XMC payloads of up to 25W of thermal dissipation. The Curtiss-Wright XF07-516 XMC for instance contains a Xilinx Kintex®-7 in addition to 4 channels of 16-bit, 250 MS/s ADC converters and is quite capable of higher power draw figures. The CHAMP-XD2M can accommodate the XF07-516, which equates to a 16 core Xeon D processor, 128 GB DDR4 memory, Xilinx Kintex FPGA, and 4 ADC channels all in a single 6U OpenVPX slot. This represents just one of hundreds of possible single-slot SWaP-optimized combinations.

Ordering Information

TABLE 1	CHAMP-XD2M ordering information
PART NUMBER	AVAILABLE OPTIONS
VPX6-483M-C14A231	› Conduction-cooled Level 100, 6U OpenVPX 1” pitch, single 16-core Xeon D (D-1587) CPU @ 1.7 GHz, 128 GB DDR4-2133, 32 GB SSD › 10/40 GigE data plane (or DDR/QDR/FDR10 InfiniBand), PCIe Gen3 expansion plane › Backplane BASE-T Gigabit Ethernet, XMC
RTM6-483-0000	Rear Transition Module (RTM) for the VPX6-483M board
CBL-483-0000	I/O break out cable for RTM of CHAMP-XD2M (VPX6-483M)
DSW-483M-001-LNX	Red Hat Linux board support package and driver suite for the Curtiss-Wright CHAMP-XD2M (VPX6-483M) Intel Xeon D 6U OpenVPX board
MNT-483M-001-LNX	Maintenance for the Red Hat Linux board support package and driver

Contact Curtiss-Wright for additional product configurations.