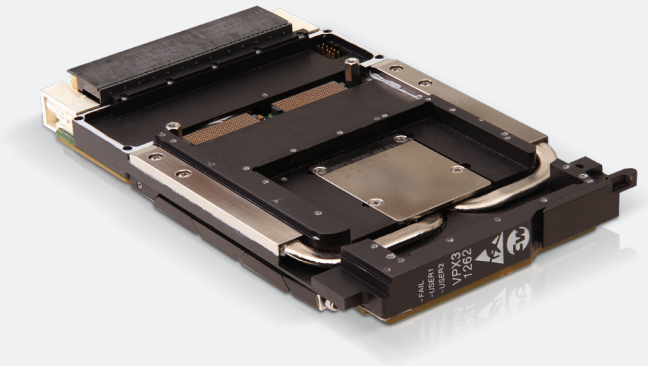
CURTISS-WRIGHT



VPX3-1262 Intel Processor

100GbE-Enabled SBC with Intel® Raptor Lake Processor Developed in Alignment with the SOSA™ Technical Standard

The VPX3-1262 from Curtiss-Wright Defense Solutions is a rugged, high performance 3U OpenVPX™ Single Board Computer (SBC) designed to meet the demanding performance needs of next-generation SOSA Aligned processing systems by combining Intel's powerful 13th Gen hybrid processor with the power and flexibility of the VPX platform's high speed fabric interconnects.

The VPX3-1262 integrates Intel's i7-13800HRE 14-core hybrid processor technology (formerly "Raptor Lake") with Curtiss-Wright's proven ruggedization technology to excel in harsh environments, making it ideal for architecting high performance computing and processing systems utilizing DSP, GPU and FPGA modules, and/or multiple SBC processors.

With a high speed, dual-channel DDR5 memory subsystem and up to 64 GB SDRAM, the VPX3-1262 maximizes the performance of the multiple processing cores, the integrated GPU cores, and the AVX2 floating-point processing units of the processor. Up to 480 GB of high-speed NVMe SSD memory make the VPX3-1262 an ideal SBC for handling applications with demanding storage, data logging and sensor processing requirements.

The VPX3-1262 includes an XMC mezzanine site to support a wide variety of expansion mezzanine daughter cards, including high performance FPGA, GPU, and storage modules. Mezzanine I/O is supported on the I/O Intensive profile variant.

Multiple Ethernet ports are provided for Control and Data Plane connectivity, supporting 10GBase-KR and 1000Base-T connectivity, and supporting Time Sensitive Networking (TSN) features.

The VPX3-1262 supports a 100G Ethernet Data Plane interface, with connectivity to 10G, 25G, 40G, and 50G link partners. For Expansion Plane connectivity, the VPX3-1262 supports PCI Express® (PCIe) operating at speeds up to Gen4 (16GT/s). The VPX3-1262 I/O Intensive variant supports a host of standard I/O including UART serial ports, SATA and USB ports, discrete DIO, and a DisplayPort interface supporting multiple displays with resolution up to 8K.

The VPX3-1262 ships with a fully featured Linux distribution and also supports Red Hat Enterprise Linux (RHEL). Other operating systems are supported through Curtiss-Wright's extensive Partnership program.

Key features

- **Developed in alignment with the SOSA Technical Standard** with variants meeting both the 3U I/O Intensive and Payload profiles
- **Fabric100™ Ecosystem Support** for 100G Ethernet in a SOSA-aligned form factor
- **Intel 13th Gen "Raptor Lake" 14-core processor**
  - + Hybrid mix of P-cores and E-cores for maximum processing efficiency
  - + Up to 64 GB DDR5 with ECC
  - + Up to 480 GB NVMe onboard SSD storage
- **High Speed Connectivity**
  - + 100G Ethernet Data Plane
  - + PCIe Gen4 Expansion Plane
  - + 10G Ethernet Control & Data Plane with TSN
- **Supports one XMC mezzanine**
- **I/O Intensive SBC adds**
  - + Base-T Ethernet, USB, SATA, UARTs, DIO
  - + DisplayPort graphics interface
  - + XMC I/O to VPX backplane

Applications

- General computing, mission processing, virtualized application hosting
- High Performance Embedded Computing (HPEC) systems
- Multi-SBC systems for advanced processing and ISR applications

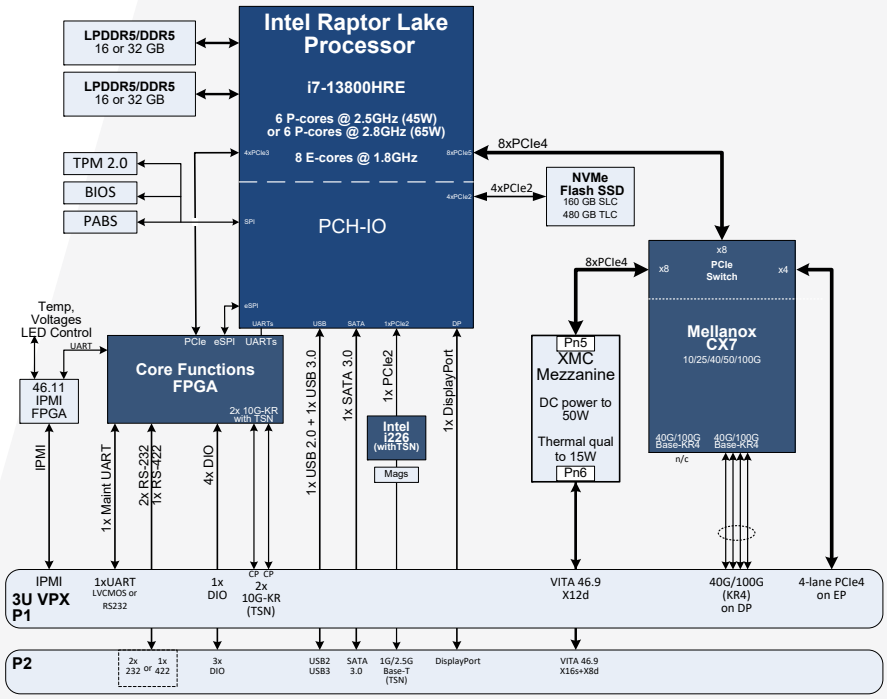


Figure 1: VPX3-1262 SBC Processor block diagram, I/O Intensive profile

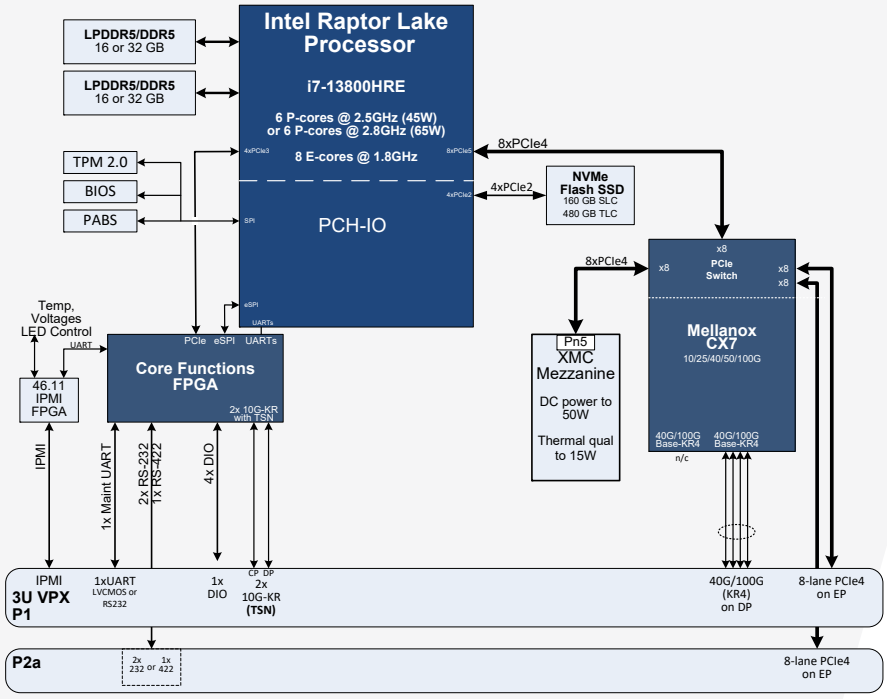


Figure 2: VPX3-1262 SBC Processor block diagram, Payload profile

Fabric100 Ecosystem

This product is a member of Curtiss-Wright's Fabric100 Ecosystem

- Offering end-to-end support for 100Gbps Ethernet fabrics, with proven performance for OpenVPX 25Gbaud signalling with reduced signal integrity risks
- Enhancing interoperability and ensuring optimal configuration of all aspects of the data fabric technology

VPX3-1262 Processor

VPX3-1262 Key Features

Powerful 13th Gen Intel i7-13800HRE CPU

The Intel i7-13800HRE (formerly “Raptor Lake”) processor is based on Intel’s industry-leading silicon technology and the latest Hybrid processor micro-architecture enhancements.

This 13th Generation processor marks the first Hybrid processor targeting embedded systems in Intel’s continual cadence for delivering the highest performance processors to the aerospace and defense industry. The processor delivers 75% more processing cores over previous generation “Tiger Lake” processors, while still meeting the same low power levels required to support today’s size, weight and power (SWaP) sensitive designs.

Aligned with the SOSA Technical Standard

After decades of dealing with proprietary point solutions, defense and aerospace organizations are facing significant interoperability, flexibility, and size, weight, power, and cost (SWaP-C) challenges on ground, air, and naval platforms. Technical standards like SOSA are designed specifically to alleviate these challenges and deliver a variety of benefits to C4ISR systems, including increased interoperability, elimination of vendor lock-in, simplified upgrades, and increased investment protection.

The VPX3-1262 is developed in alignment with the SOSA Technical Standard, with variants supporting both the 3U I/O Intensive SBC PIC profile and the 3U Payload Processor PIC profile. Click here to learn more about SOSA.

Hybrid Processor Architecture

The VPX3-1262 supports Intel’s Hybrid processor architecture, developed to meet the most demanding workload requirements by directing applications requiring high performance to higher performance P-cores, while utilizing higher efficiency E-cores for less time-critical processing needs.

The i7-13800HRE processor offers 6 x hyper-threading P-cores (12 x threads) plus 8 x E-cores for a total of 14-cores and 20-threads. P-cores offer the highest performance to handle complex workloads and E-cores excel at supporting multi-threading operations and lower priority tasks. All processing cores operate simultaneously.

Read more about Intel Hybrid Architectures here:
Hybrid Architecture (intel.com)

Curtiss-Wright has developed informative White Papers detailing the performance and efficiencies of Hybrid processors, with example use-cases that greatly benefit the embedded Aerospace and Defense industry. These White Papers can be found here: <TBD>

Power Consumption and CPU Tuning

The VPX3-1262 provides extremely flexible and dynamic methods of controlling power consumption. From statically parking cores in the UEFI/BIOS to dynamically adjusting CPU clocks and core affinity at run time, the VPX3-1262 performance can be tailored to meet a wide range of processing and power requirements. The Intel CPU power consumption can range from 5 watts to 45 watts, and a higher-performance 65 watt mode can be configured for even higher performance applications.

Dual Data Rate (DDR5) SDRAM

The VPX3-1262 has two independent 64-bit DDR5 SDRAM memory banks and can be fitted with 32 or 64 GB total capacity. The DDR5 interface operates at 4,800 MT/s, yielding a memory throughput performance of 76.8 GB/s.

To preserve data integrity, the SDRAM is protected with in-band error-correction (ECC) circuitry.

NVMe SSD

The VPX3-1262 is configured with high-performance Non-Volatile Memory Express (NVMe) local storage connected directly to the processor’s PCIe interface, eliminating traditional performance bottlenecks associated with SATA connected storage. The module is configured with a single 160 GB SSD operating in SLC mode with the highest P/E cycle endurance. For applications requiring higher capacity storage, a 480 GB SSD can be fitted operating in TLC mode with reduced P/E cycle endurance.

Fabric Ports

The VPX3-1262 offers a 100GbE Ethernet Data Plane, supporting a 100GBASE-KR4 interface. The Data Plane can also support 40GBASE-KR4, as well as single lane 10GBASE-KR and 25GBASE-KR and dual-lane 50GBASE-KR2 interfaces. Data Plane ports support RoCE V2 for line-rate performance without loading down the Intel processor. The devices also support OpenMPI, OFED and GPUDirect, with available 3rd party and community software.

On the Expansion Plane, the VPX3-1262 provides PCIe connections, used primarily to connect at the highest possible speeds to adjacent VPX modules. The I/O Intensive variant offers 4-lanes of PCIe, and the Payload profile variant offers both an 8-lane variant (without P2) and/or a 16-lane (with P2a) variant.

The PCIe port operates at Gen1 (2.5 GT/s), Gen2 (5 GT/s), Gen3 (8 GT/s) and Gen4 (16 GT/s) speeds, for extremely fast data transfers.

Common uses of the VPX Expansion Plane are to connect the processor to sensor or signal acquisition modules, to augment the processor with additional graphics modules, or to connect to dedicated GPU or FPGA modules offering additional computational power. The Expansion Plane can also connect to a central PCIe switch permitting PCIe expansion or high-speed data communications across the PCIe fabric.

Control and Data Plane Ethernet interfaces

The VPX3-1262 offers two SerDes Ethernet ports supporting 10GBASE-KR (10 GbE) with auto-negotiation supporting 1000BASE-KX (1 GbE) operation.

The VPX3-1262 I/O Intensive variant adds an additional 1000BASE-T port.

These ports offer a range of Time Sensitive Networking (TSN) features, which adds real-time deterministic messaging capabilities to standard Ethernet networks. To make use of TSN features, a TSN capable Ethernet switch is required, such as the Curtiss-Wright VPX3-6826.

XMC Site

The module is equipped with one mezzanine site capable of supporting VITA XMC mezzanine modules. The XMC site supports eight lanes of PCIe with data rates up to Gen4. To enhance signal integrity with high-speed mezzanines, the module supports low-insertion force VITA 61 connectors. Contact Curtiss-Wright for VITA 42 ordering options.

On the I/O Intensive variant, Pn6 I/O to the backplane is provided per VITA 46.9 as P1w9-X12d+P2w9-X16s+X8d providing 20 pairs of high-speed differential I/O and 16 single-ended signals from the mezzanine site to the VPX backplane connector. The Payload variant has no Pn6 I/O to the backplane and can still host a PCIe connected XMC mezzanine such as an FPGA, a GPU, or an expanded storage module.

The mezzanine sites adhere to the VITA 20-2001 (R2005) conduction-cooled PCI Mezzanine Card mechanical standard. To optimize the thermal transfer from XMC modules to the base card, the VPX3-1262 thermal frame incorporates both the primary and secondary thermal interfaces as defined by VITA 20-2001 and support direct thermal shunting from the mezzanine to the VPX3-1262 thermal frame.

Serial Ports

The VPX3-1262 provides one UART maintenance port operating at LVCMOS levels. A factory build option can configure this port to operate at RS-232 levels. The I/O Intensive variant provides additional configurable serial ports operating as a single RS-422 or dual RS-232 ports.

All serial ports support asynchronous communications with common baud rates configurable from 300 to 115,200 baud. The RS-422 port also supports high-speed operation up to 460,800 baud with selectable termination.

Discrete Digital I/O (DIO)

The VPX3-1262 provides independent discrete digital I/O signals. Each DIO is individually programmable as an input or an output. DIO's are capable of triggering an interrupt upon a change of state and are programmable to detect either rising or falling edge. All DIOs are 5V-tolerant.

The I/O Intensive variant supports four DIO signals, and the Payload profile variant supports one DIO signal.

USB Ports

The VPX3-1262 I/O Intensive variant provides one USB 2.0 and one USB 3.2 Gen1 port.

SATA Ports

The VPX3-1262 I/O Intensive variant provides one SATA 3.0 interface on the rear VPX backplane operating at up to 6 Gbps.

Display Interface

The processor supports an integrated Intel Iris Xe graphics engine, which operates with a base clock of 350 MHz, increasing up to 1.5 GHz for high-performance display operations.

The VPX3-1262 I/O Intensive variant provides one 4-lane DisplayPort interface to the backplane and supports DisplayPort modes at up to HBR3 data rates with resolutions up to 8K60 with HDR.

Table 1: DisplayPort Graphics Resolution

Display Configuration	Signal Rate (per lane)	Effective Data Rate (4-lane)	Max Resolution
DP 1.1 (HBR)	2.7 Gbps	8.64 Gbps	2560 x 1440 @ 75 Hz
DP 1.2 (HBR2)	5.4 Gbps	17.28 Gbps	3840 x 2160 @ 75 Hz
DP 1.4 (HBR3)	8.1 Gbps	25.92 Gbps	7680 x 4320 @ 60Hz

Up to three independent displays can be fed from the single DisplayPort interface when configured for Multi-Stream Transport (MST) operation.

Integrated GPU

The integrated graphics engine can also provide general purpose GPU functionality, offering up to <TBD> GFLOPS of performance and usable by applications using an OpenCL programming interface.

Integrated Hardware CODEC

The processor incorporates a hardware video codec, accelerating video compression and decompression algorithms and reducing CPU processing requirements. The codec supports MPEG, H.264 (AVC), H.265 (HEVC) and VP9 formats and features both 8-bit and 10-bit (HDR) image processing. Accelerated codec features are supported by Intel Media Studio tools.

Temperature Sensors

The VPX3-1262 provides temperature sensors to measure board and processor temperatures. There is a sensor at each edge of the card and sensors built into the CPU. All temperature sensors can be read by software.

Timers

The processor includes multiple general purpose and high-resolution timers as well as a hardware watchdog timer. Software can select whether a watchdog exception event causes a software interrupt, a processor reset, a card reset, or a system reset.

Security Features

The VPX3-1262 is equipped with Trusted Computing features to protect against physical and remote attacks. For more information, see our TrustedCOTS™ brochure. Due to the nature of trusted computing, not all security features are described here. Please contact Curtiss-Wright for additional security information.

Trusted Platform Module (TPM) support

The VPX3-1262 includes a Trusted Platform Module (TPM) 2.0 hardware security device which is compliant to FIPS-140-2 and is Common Criteria certified. The TPM can be used to create a secure computing environment, ensuring only trusted and signed UEFI firmware (aka BIOS) and software can execute on the board.

The TPM supports secure key storage, advanced cryptography algorithms, and other enhanced features.

Intel Boot Guard (BtG)

The VPX3-1262 supports Intel Boot Guard (BtG), which provides both an authenticated and a measured boot. With Boot Guard enabled, only signed and authenticated boot modules can be executed, creating a secure Root-of-Trust (RoT) on the module. Modules can be provisioned and preloaded with BootGuard signed firmware from the factory, simplifying the setup of a secure computing solution.

UEFI Secure Boot

In addition to Intel-specific Boot Guard security features, the VPX3-1262 includes full support for UEFI Secure Boot. Secure Boot extends the secure boot process to validate the operating system boot loader, and then extends security into the operating system.

Software Support

The VPX3-1262 is supported by a suite of firmware, operating systems, and RTOS board support packages (BSP), as well as communication and signal processing libraries. Systems developers will be able to kick-start application development using a common set of features and software interfaces across many products from Curtiss-Wright.

Built-in Test (BIT)

Built-in Test (BIT) is a library of diagnostic routines to support Power-On BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) for health management of the module. BIT operations are supported through BIOS and software APIs and can be integrated into customer developed applications.

- PBIT for power-up self-test
- IBIT for user-initiated self-test
- CBIT for continuous self-test and monitoring

Operating System Software

The VPX3-1262 is shipped with CentOS Linux preloaded from the factory. A separate BSP can be purchased to support Red Hat Enterprise Linux (RHEL) which includes full Linux driver source code.

Rear Transition Module

For building development systems in a lab environment, Curtiss-Wright provides a Rear Transition Module which plugs into the backside of the VPX3-1262's backplane and provides access to many of the board I/O interfaces on industry standard connectors.

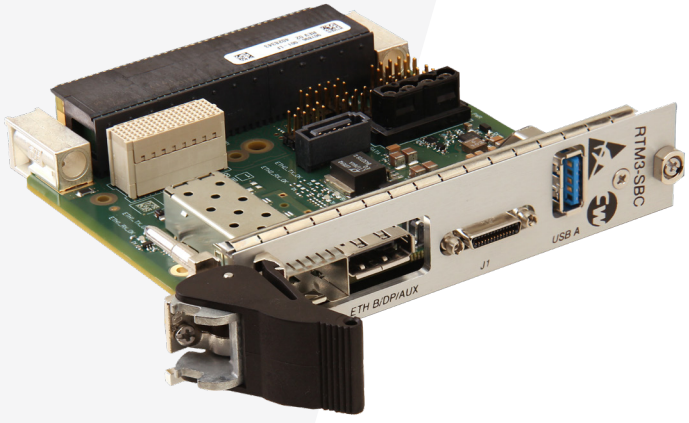


Figure 3: Rear Transition Module

VPX Slot Profiles

The VPX3-1262 is offered in two popular SOSA-aligned profiles to meet the needs of a wide variety of system applications.

The SOSA I/O Intensive Profile is shown in Figure 4. Meeting the VITA slot profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16, this profile populates the entire VPX connector with copper connectors to offer the widest selection of interfaces, and supports XMC mezzanine I/O.

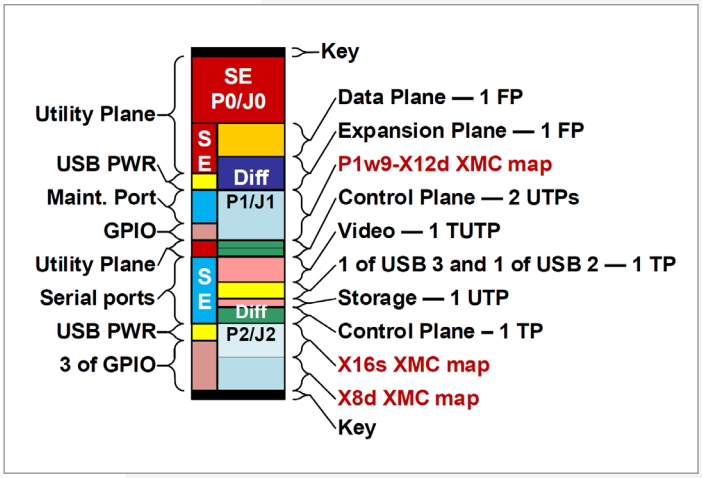


Figure 4: VITA/SOSA Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

Two variants are available meeting the SOSA Payload Profile. Figure 5 shows the VITA slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11 and features an 8-lane PCIe Expansion Plane with a full P2 aperture. Figure 6 shows the VITA slot profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.13 which features a 16-lane PCIe Expansion Plane with P2A populated and P2B aperture.

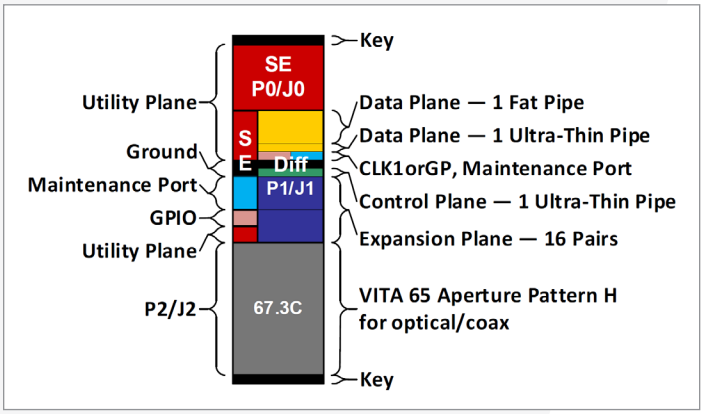


Figure 5: VITA/SOSA Profile SLT3-PAY-1F1U1S1S1U1U2F1H-14.6.11

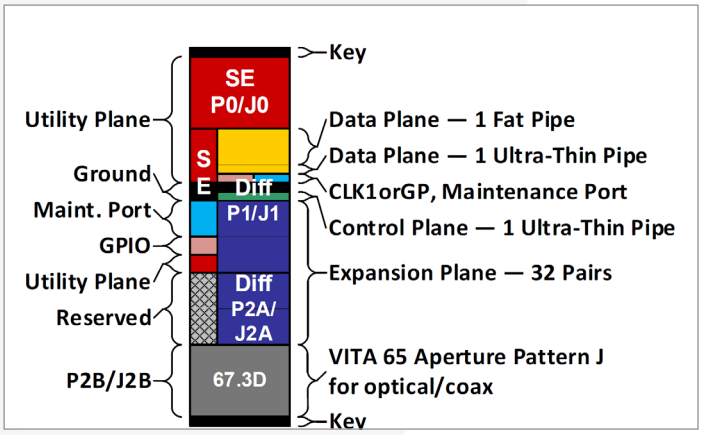


Figure 6: VITA/SOSA Profile SLT3-PAY-1F1U1S1S1U1U4F1J-14.6.13

The board draws primary power from the VPX Vs1 (+12V) power rail only.

Specifications and Standards

Form Factor

- 3U OpenVPX, developed in alignment with the SOSA Technical Standard
  - I/O Intensive SBC profile:
    - SLT3-PAY-1F1F2U1TU1T1U1T -14.2.16
    - MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-4, -<TBD>[1]
  - Payload PIC profile (no P2):
    - SLT3-PAY1F1U1S1S1U1U2F1H -14.6.11
    - MOD3-PAY-1F1U1S1S1U1U2 4F1H-16.6.11-11, -<TBD>[1]
  - Payload PIC profile (with P2A):
    - SLT3-PAY-1F1U1S1S1U1U2F1H -14.6.13
    - MOD3-PAY-1F1U1S1S1U1U2F1H -16.6.13-1, -<TBD>[1]

Processor

- 13th Gen Intel i7-13800HRE (formerly “Raptor Lake”) processor
  - 14-core / 20-thread processor, 45W or 65W TDP configurable
    - 6 x P-cores at 2.5 GHz (45W) or 2.8 GHz (65W) base clock, turbo to 5.0 GHz
    - 8 x E-cores at 1.8 GHz base clock, turbo to 4.0 GHz
  - Intel Advanced Vector Extensions (AVX, AVX2) floating-point
  - Intel Virtualization Technology (VT-x, VT-d)
  - Intel AI Acceleration with Deep Learning Boost (VNNI)
  - Intel Iris Xe Graphics with 96 EUs
  - Intel Multi-Key Total Memory Encryption (MK-TME)

SDRAM Memory

- 32 or 64 GB DDR5 at 4,800 MT/s
- Dual-channel memory configuration with IB-ECC and supporting MK-TME encryption

Non-Volatile Memory

- 160 or 480 GB NVMe SSD storage
  - 160 GB capacity in SLC mode
  - 480 GB capacity in TLC mode

32 MB SPI flash for BIOS functions with PABS recovery

Expansion Plane fabric

- 4-lane (I/O Intensive) or 8/16-lane (Payload) PCIe Gen4 Expansion Plane

Data Plane Ethernet Interface

- 1 x Data Plane fat-pipe interface supporting the following Ethernet port configurations:
  - 1 x 40G-KR4 or 100G-KR4 port
  - 2 x 50G-KR2 ports
  - 4 x 10G-KR or 25G-KR ports

DP/CP Ethernet Ports

- 2 x 10GBASE-KR also supporting 1000BASE-KX operation
- 1 x 1000Base-T (I/O Intensive)
- These Ethernet ports support the following TSN features:
  - 802.1AS-2020 Time synchronization for TSN
  - 802.1Qav Forwarding and queuing enhancements (credit-based shaping)
  - 802.1Qbv Time-aware shaping
  - 802.1Qbu, 802.3br Frame pre-emption
  - 802.1Qcc via Linux TSN software stack
- SerDes 10GBASE-KR ports support the following additional TSN features
  - 802.1Qcr Asynchronous traffic shaping
  - 802.1CB Frame replication
  - 802.1Qci Per-stream filtering and policing

XMC Mezzanine Site

- 8-lane PCIe Gen4 XMC mezzanine
  - Low insertion force VITA 61 (XMC 2.0) connectors
    - VITA 42 connectors also available upon request
  - I/O Intensive profile supports backplane Jn6 I/O mapping P1w9-X12d+P2w9-X16s+X8d
- Support for up to 50 watts DC power available
- Thermal qualification with 15 watt mezzanines. Contact Curtiss-Wright for higher power mezzanine qualification details

Additional I/O

All variants:

- 1 x UART maintenance port LVCMOS signal levels (RS-232 also available)
- 1 x Discrete (+5V tolerant) I/O
- 1 x USB 2.0 port

I/O Intensive SBC profile adds:

- 3 additional discrete I/O
- 2 x RS-232 or 1 x RS-422 serial UART channels
- 1 x USB 3.2 Gen1 (5 Gbps)
- 1 x SATA 3.0 port
- 1 x DisplayPort interface supporting up to HBR3 rates

Health Management

- IPMC per VITA 46.11 for all Tier 1 and Tier 2 requirements
- SOSA extensions

Security Features

- Trusted Platform Module (TPM) 2.0 hardware device, compliant to FIPS and Common Criteria
- Intel Boot Guard, authenticated and measured boot (contact factory)
- UEFI Secure Boot
- SSD encryption (optional)
- Intel MK-TME Multi-Key Total Memory Encryption

[1] <TBD> profiles are not yet defined by VITA, and will support 100GbE Data Plane, and PCIe Gen4 Expansion Plane

Software Support

- Shipped with CentOS Linux pre-loaded from the factory
- A separate BSP can be purchased to support Red Hat Enterprise Linux (RHEL) and includes full Linux driver source code

Built-in Test

- Power-up BIT (PBIT)
- User Initiated BIT (IBIT)
- Continuous BIT (CBIT)

Power

- Primary Power: Vs1 (+12V), 3.3V_AUX
- RTC Power from VBAT

Power Consumption

- Power consumption will vary based on operational loading. Values below are guidelines for operation with 14 cores @ base frequencies at room temperature (25°C) – contact Curtiss-Wright for more details on power consumption.
- Idle power consumption = <TBD> watts
- Typical power consumption = <TBD> watts
- Maximum power consumption = <TBD> watts
- Note: power consumption is exclusive of optional mezzanine power

VPX Connectors

- P0 = RT2 connectors
- P1, P2 = RT3 connectors

Environmental

- Conduction-cooled: Level 300 with 2LM covers
  - Designed to meet VITA 47.3 ECC3SL1
- For additional cooling methods, such as Air-Cooled, Air Flow-Through, LFT/FFT, etc, please contact Curtiss-Wright

Weight

- Conduction-cooled Level 300: TBD

Ordering Information

VPX3-1262 modules described in this product sheet are orderable per below.

- All VPX3-1262 modules listed are conduction-cooled, L300 with 2LM covers
- Rear Transition Modules (RTM3-SBC) are air-cooled and support lab development

Table 2: VPX3-1262 Ordering Information, I/O Intensive Profile

Part Number	Description
VPX3-1262-C252E50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, I/O Intensive Profile – **32 GB DRAM**, 160 GB SSD, high-performance thermal frame
VPX3-1262-C252G50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, I/O Intensive Profile – **64 GB DRAM**, 160 GB SSD, high-performance thermal frame
RTM3-SBC-0002	Rear Transition Module aligned with the SOSA Technical Standard, I/O Intensive Profile – Provides breakout connectors and cables to most I/O interfaces – Supports Curtiss-Wright RIM mezzanine module for XMC I/O breakout › RIM-GEN-0001 for low-speed signals › RIM-GEN-0002 for high-speed and differential signals

Table 3: VPX3-1262 Ordering Information, Payload Profile

Part Number	Description
VPX3-1262-C253E50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, Payload Profile, **no P2** – **32 GB DRAM**, 160 GB SSD, high-performance thermal frame
VPX3-1262-C253G50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, Payload Profile, **no P2** – **64 GB DRAM**, 160 GB SSD, high-performance thermal frame
RTM3-SBC-1001	Rear Transition Module aligned with the SOSA Technical Standard, Payload Profile, **no P2** – Provides breakout connectors and cables to most I/O interfaces
VPX3-1262-C255E50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, Payload Profile, **with P2a** – **32 GB DRAM**, 160 GB SSD, high-performance thermal frame
VPX3-1262-C255G50	Intel 13th Gen Raptor Lake i7-13800HRE Single Board Computer, Payload Profile, **with P2a** – **64 GB DRAM**, 160 GB SSD, high-performance thermal frame
RTM3-SBC-1011	Rear Transition Module aligned with the SOSA Technical Standard, Payload Profile, **with full P2** – Provides breakout connectors and cables to most I/O interfaces

Table 4: Software and Accessories ordering information

Part Number	Description
DSW-1262-6xy0-RHL6	Red Hat Enterprise Linux (RHEL) X.Y BSP for VPX3-1262 Also supports CentOS Linux. Includes driver source code
MNT-1262-LNX	Annual maintenance and Software Upgrade Program (SUP) for VPX3-1262 Linux
SVC-1262-BTG-NEW SVC-1262-BTG-NEWCW	VPX3-1262 BootGuard New Customer Package Provides signed boot firmware for authenticated and measured boot via Intel BootGuard Includes signing of the UEFI firmware (aka: BIOS) with a customer generated security key (BTG-NEW) or with a Curtiss-Wright generated and managed security key (BTG-NEWCW)

SOSA™ Sensor Open Systems Architecture

MEMBER VITA Open Standards, Open Markets