Qbit Labs Private Limited
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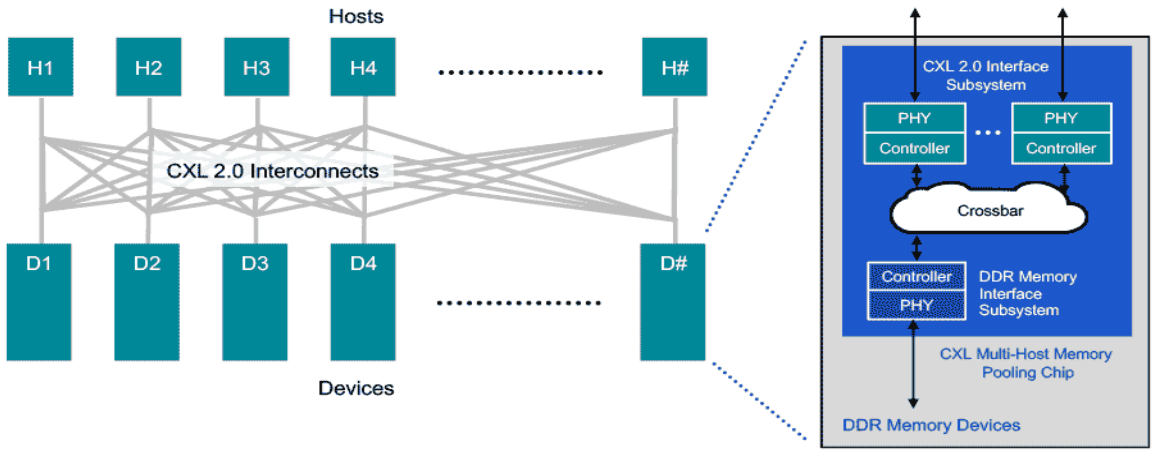
CIN NO. U29309DL2020PTC363015

CXL 2.0

Introduction

Compute Express Link (CXL) 2.0 is an advanced interconnect standard designed to enable high-speed, low-latency communication between processors, memory, and accelerators in data centers and high-performance computing environments. Building on the foundation of CXL 1.1, it introduces key features like memory pooling, switching, and multi-level fabric support, enabling more efficient resource sharing and scalability. With backward compatibility and support for emerging workloads, CXL 2.0 is paving the way for a new era of composable infrastructure and efficient data center architectures.

Architectural Overview



Component	Description
Hosts (H1, H2, H3, H4)	Compute nodes or processors communicating via the CXL 2.0 interconnect.
Devices (D1, D2, D3, D4)	CXL devices such as accelerators, memory modules, or pooled resources.
CXL 2.0 Interconnects	High-speed, low-latency links enabling communication between hosts and devices.
Switching Fabric	Multi-host support through centralized switching for resource sharing.
Multi-Host Memory Pooling Chip	Enables dynamic memory allocation across hosts using a crossbar design.
CXL Subsystem	Contains PHY and controllers managing communication and resource access.
DDR Memory Devices	Back-end memory interfaced via the CXL multi-host memory pooling chip.

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Specifications

SN	Specification	Details
1.	CXL Version	2.0
2.	Supported Protocols	CXL.io, CXL.memory, CXL.cache
3.	Backward Compatibility	Fully backward compatible with CXL 1.1 and CXL 1.0
4.	Data Rate	Up to 32 GT/s (Giga transfers per second)
5.	Link Widths	x4, x8, and x16 link widths supported
6.	Supported Interfaces	PCIe Gen 5
7.	Memory Types Supported	DRAM, Persistent Memory, and emerging memory technologies
8.	Key Use Cases	Memory pooling, memory sharing, accelerators, and persistent memory
9.	Topology Enhancements	Support for multi-level switching, memory pooling, and device sharing
10.	Coherency	Cache and memory coherency between host processor and accelerators
11.	Switching	Supports up to 16 logical devices through a single CXL port
12.	Fabric Management	Supports flexible and scalable device interconnect for dynamic system reconfiguration
13.	Error Handling	Enhanced error isolation and recovery
14.	Encryption and Security	Improved security with protocol enhancements and support for memory encryption
15.	Device Hot-Plug	Support for hot-plugging of devices
16.	Physical Interface	Uses PCIe 5.0 physical interface
17.	Latency	Ultra-low latency interconnect for high-performance workloads
18.	Power Management	Integrated with PCIe power management features
19.	Security	Supports enhanced security protocols for encryption and access control
20.	Memory Pooling	Allows multiple hosts to access shared memory resources