Qbit Labs Private Limited
104, FF, Iris Tech Park, Sector 48
Sohna Road, Gurugram,122018
CIN NO. U29309DL2020PTC363015

CXL 3.0

Introduction

CXL (Compute Express Link) 3.0 is a high-speed interconnect standard that enhances data center performance with up to 64 GT/s data rates. It enables memory pooling for efficient resource sharing, reduces latency, and supports multiple protocols over a single interface. Scalable for workloads like AI and data analytics, CXL 3.0 is also backward compatible, ensuring easy integration into existing systems. Overall, CXL 3.0 significantly improves the performance and efficiency of modern computing architectures.

Features

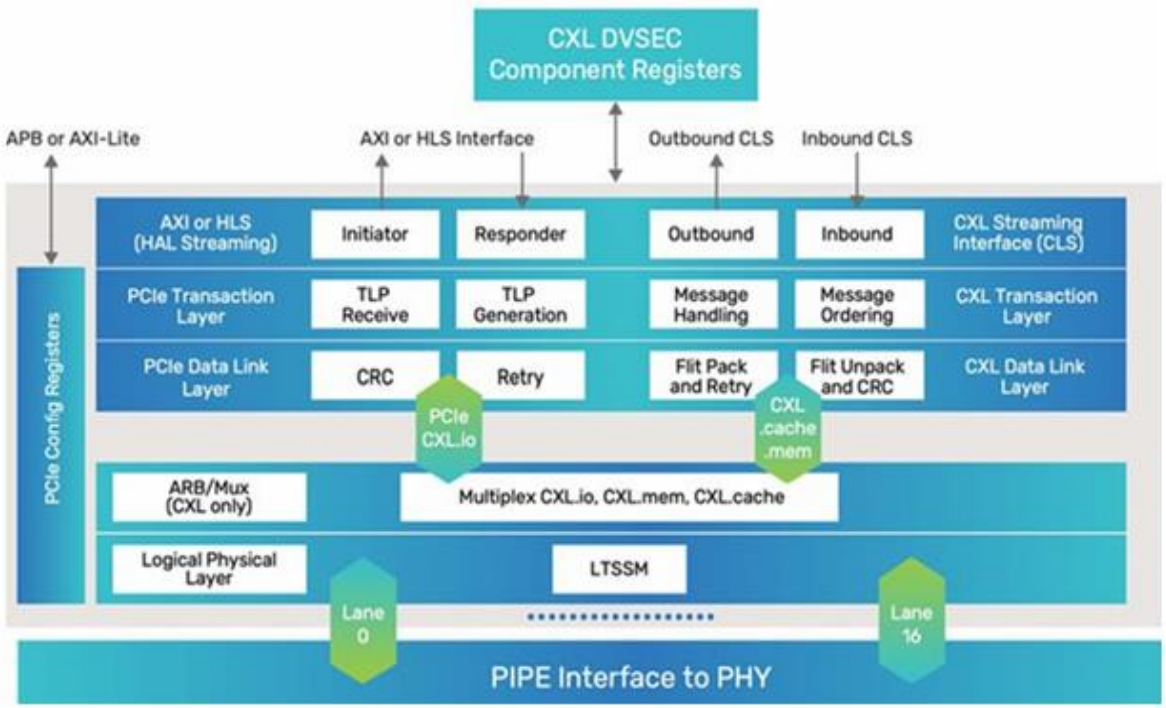
1. Doubles the bandwidth of CXL 2.0 with PCIe 6.0 support.
2. Supports multi-level memory pooling for efficient resource utilization.
3. Enables devices to share resources across multiple hosts.
4. Allows direct communication between devices without host intervention.
5. Supports switching and fabric management for larger and complex deployments.
6. Compatible with previous CXL versions and PCIe standards.
7. Offers ultra-low latency for compute-intensive applications.
8. Incorporates improved encryption and authentication mechanisms.

Specifications

SN	Specification	Details
1.	CXL Version	3.0
2.	Supported Protocols	CXL.io, CXL.cache, CXL.memory
3.	Interconnect	PCIe 6.0
4.	Data Rate	Up to 64 GT/s per lane
5.	Link Width	x1, x2, x4, x8, x16, x32
6.	Maximum Memory Capacity	Up to 2 TB
7.	Latency	Sub-microsecond
8.	Maximum Bandwidth	512 GB/s (up to 8 lanes at 64 GT/s)
9.	Error Correction	ECC, CRC, Replay Buffer
10.	Memory Interleaving	Fine-grained
11.	Virtualization	SR-IOV, MR-IOV
12.	Operating Temperature	Range – 40°C to 85°C
13.	Lane Count	1 to 8 lanes
14.	Memory Types Supported	DRAM, Non-Volatile Memory (NVM)
15.	Forward Compatibility	Supports CXL 2.0 and CXL 1.1
16.	Hot-Plug Support	Yes
17.	Cache Line Size	Configurable cache line sizes (e.g., 64B, 128B)
18.	Topology	Point-to-point, switchable, multi-host
19.	Security	Built-in mechanisms for secure data transfer and authentication
20.	Power Efficiency	Optimized for low power consumption during high-throughput operations

Qbit Labs Private Limited
104, FF, Iris Tech Park, Sector 48
Sohna Road, Gurugram,122018
CIN NO. U29309DL2020PTC363015

Architectural Overview



This architecture is designed to enhance data processing performance by enabling high-speed connections between CPUs, GPUs, and memory devices

1. **CXL DVSEC Component Registers**: Holds configuration and control information for managing CXL-specific functions.
2. **AXI/HLS Interface**: Handles **initiator** and **responder** operations for host-device communication.
3. **CXL Streaming Interface (CLS)**
    - **Outbound/Inbounds CLS:** Manages message handling, ordering, retries, and CRC.
4. **CXL Transaction & Data Link Layers:** Ensures reliable data exchange with error checks (CRC) and retry mechanisms.
5. **PCIe Integration**
    - **PCIe Transaction and Data Link Layers:** Manage PCIe transactions for interoperability with PCIe devices.
    - **Multiplexing:** Dynamically switches between CXL I/O, CXL Memory, and CXL Cache protocols.
6. **Logical Physical Layer**: Handles signal integrity and low-level data transfer. Includes the **LTSSM** for establishing and maintaining link integrity.
7. **PIPE Interface to PHY**: Physical layer interface connecting lanes (e.g., Lane 0 to Lane 16) for high-speed data transmission.
8. **Arbitration and Muxing**: Manages resource sharing and protocol-specific priorities between CXL operations.