Qbit Labs Private Limited
104, FF, Iris Tech Park, Sector 48
Sohna Road, Gurugram,122018
CIN NO. U29309DL2020PTC363015

DSI-2

Introduction

DSI-2 (Display Serial Interface version 2) is a high-speed serial interface standard primarily used in mobile and embedded systems for connecting processors to display devices like LCDs and OLEDs. It is a part of the MIPI (Mobile Industry Processor Interface) standards and bandwidth, offers improved power efficiency, and scalability compared to its predecessor, DSI-1. DSI-2 supports higher resolutions, refresh rates, and advanced features like command mode and video mode transmission, making it ideal for modern devices with high-performance display requirements, such as smartphones, tablets, and automotive displays.

Features

1. Supports up to 4.5 Gbps per lane for high-resolution displays.
2. Configurable up to 4 lanes for increased data throughput.
3. Fully compatible with DSI-1 for seamless integration.
4. Optimized signaling for reduced power consumption.
5. Includes command and video modes for versatile display types.
6. Integrated error correction and packet retransmission capabilities.
7. Supports adaptive resolution and refresh rates for better performance.

Specifications

SN	Specification	Details
1.	Standard	DSI-2 (Compliance with MIPI DSI standards)
2.	Interface Type	Mobile Industry Processor Interface (MIPI)
3.	Maximum Data Rate	Up to 6 Gbps
4.	Number of Data Lanes	1 to 4
5.	Lane Speed	Up to 1.5 Gbps per lane
6.	Pixel Format	RGB888, RGB666, RGB565, Grayscale
7.	Video Modes	Video mode and Command mode
8.	Resolution Support	Up to 2560 x 1600 (WQXGA)
9.	Power Consumption	Low power consumption with dynamic scaling
10.	Connector Type	Varies (typically micro-coax or flat flexible cable)
11.	Control Signals	Includes HSYNC, VSYNC, DE (Data Enable)
12.	Clocking	Clock-less operation; relies on embedded clocking
13.	Backlight Control	Supported via I2C or PWM signals
14.	Signaling Type	Low-Voltage Differential Signaling (LVDS)
15.	Refresh Rates	Supports dynamic refresh rates for performance tuning
16.	Error Handling	Error detection with packet retransmission

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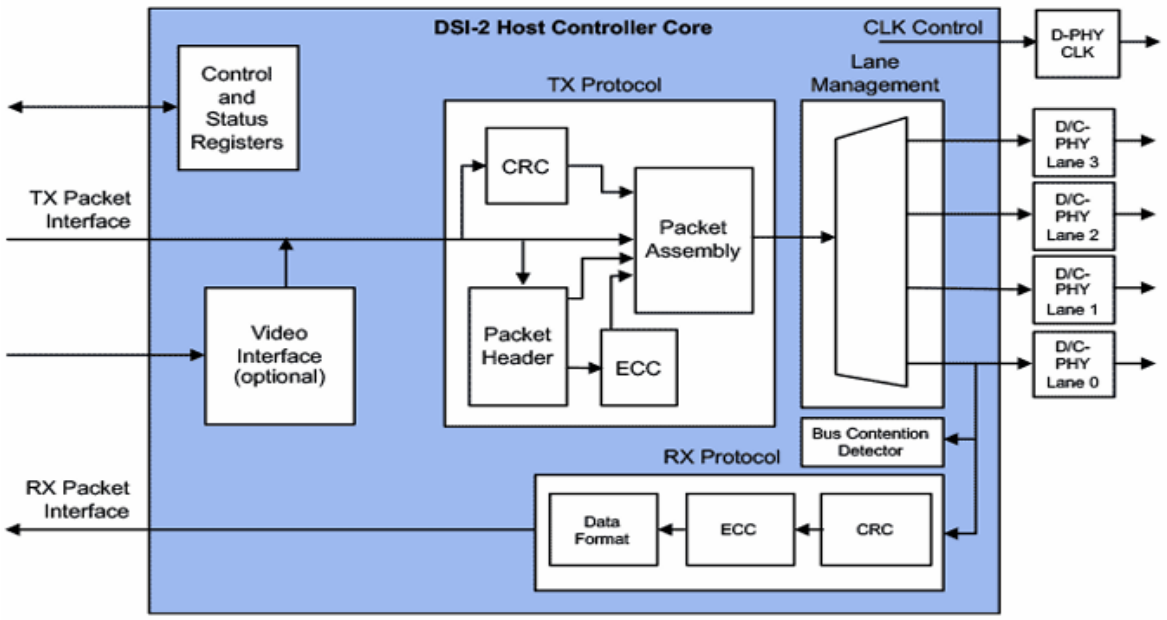
Architectural Overview



This modular architecture ensures high-speed, reliable communication for both command and video mode operations in the DSI-2 interface.

1. **Control and Status Registers**: Manages configuration, control, and status reporting of the DSI-2 interface.
2. **Video Interface (Optional)**: Supports optional integration for video data streams.
3. **TX Packet Interface**: Responsible for transmitting packetized data to the PHY layers.
4. **TX Protocol Components**: It contains **CRC** to ensures data integrity by detecting errors, **Packet Assembly** to assembles packets with headers and payloads for transmission, and **Packet Header & ECC** to adds headers and performs error correction for reliable communication.
5. **RX Packet Interface**: Receives packetized data from the PHY layer.
6. **RX Protocol Components**: It contains **Data Format** to processes received data for formatting and interpretation, **ECC** to detects and corrects errors in incoming data, and **CRC** to verifies the integrity of received packets.
7. **Lane Management**: Handles the management of up to 4 D/C-PHY lanes for data transmission and reception.
8. **Bus Contention Detector**: Detects conflicts or errors on shared communication channels.
9. **CLK Control**: Synchronizes operations between the host controller core and the PHY layers.
10. **D/C-PHY Lanes (0–3)**: Physical data transmission lanes that use Low-Voltage Differential Signaling to interface with display components.