

VPX3-1222/V3-1222 Avionics Processor

Safety Certifiable Processor Board with 13th Gen Intel® Core™ i7

The Curtiss-Wright V3-1222 rugged, high performance 3U OpenVPX™ Single Board Computer (SBC) was designed for systems targeting Design Assurance Level (DAL) A using AC/AMC 20-152A as a means of compliance (includes guidance on the use of DO-254). The VPX3-1222/V3-1222 Processor combines the powerful 13th Gen Intel® Core™ i7-1376PRE performance hybrid architecture and integrated Iris® X^e graphics to excel at demanding performance and graphics needs of next-generation safety certifiable processing systems with the power and flexibility provided by industry standard SOSA™ aligned VPX platform.

The VPX3-1222/V3-1222 avionics processor card integrates the Intel i7-1376PRE low power 14-core hybrid processor technology (formerly “Raptor Lake”) with Curtiss-Wright’s proven safety certifiable COTS development process and ruggedization technology to excel in harsh environments.

With a 64 GB high speed, dual-channel LPDDR5 memory subsystem, the V3-1222 processor maximizes the performance of the multiple processing cores with integrated GPU cores.

In place of an XMC mezzanine site, the VPX3-1222/V3-1222 processor board provides additional built-in interfaces to enable broad system use case support such as 1000BASE-T Ethernet, DisplayPort graphics Interface, DIO, I2C and PCI Express® (PCIe).

Multiple Ethernet ports are provided for Control Plane connectivity, supporting 10GBASE-KR and 1000BASE-T connectivity, and supporting Time Sensitive Networking (TSN) features.

For Expansion Plane connectivity, the VPX3-1222/V3-1222 supports PCIe operating at speeds up to Gen3. The VPX3-1222/V3-1222 supports a host of standard I/O including UART serial ports, USB ports, discrete DIO, and a DisplayPort interface supporting multiple displays with resolutions up to 4K.

For secure computing environments, the VPX3-1222/V3-1222 includes Intel’s trusted computing capabilities through the inclusion of a Trusted Platform Module (TPM) 2.0.

Key Features

- Developed to meet AC 20-152A/AMC 20-152A Design Assurance (DAL) A process assurance
- Aligned with the SOSA Technical Standard to meet the 3U I/O Intensive Profile
- 13th Gen Intel® Core™ i7-1376PRE “Raptor Lake” 14-core processor
 - Hybrid mix of P-cores and E-cores for maximum processing efficiency
 - 64 GB LPDDR5 with 1B-ECC
 - 160 GB SSD
 - Slim bootloader for fastest boot times
- Connectivity
 - PCIe Gen3 Expansion Plane
 - 10G Ethernet Control & Data Plane
 - Quad 1000BASE-T Ethernet with TSN
 - USB, UARTs, DIO, I2C
 - Dual DisplayPort graphics interface
- Graphics Driver Support
 - Vulkan SC
 - OpenGL SC 2.0

Applications

- Primary Flight Displays
- Flight Control Computer
- Advanced Flight Computing (Autonomous)
- Safety Critical Mission Processing
- Degraded Visual Environment Processing

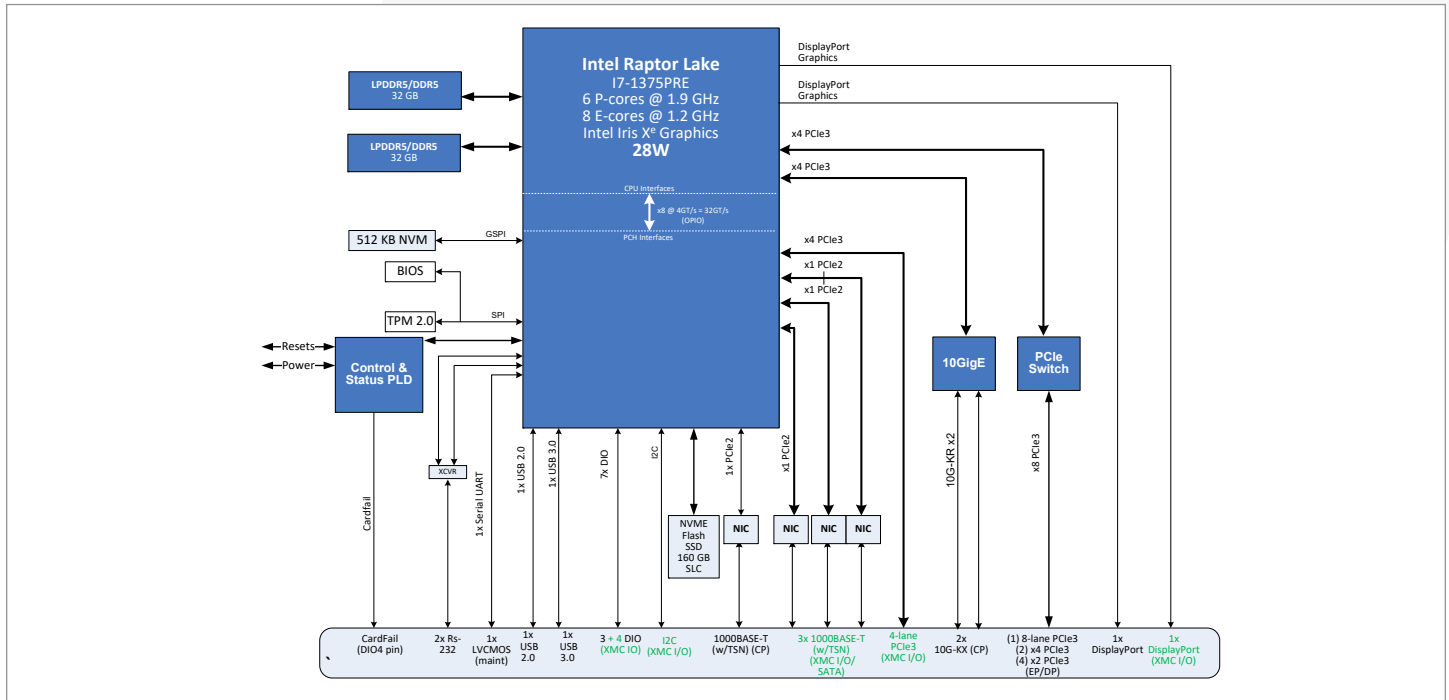


Figure 1: VPX3-1222/V3-1222 SBC processor block diagram

Key Features

Powerful 13th Gen Intel Core i7-1376PRE CPU

The Intel Core i7-1376PRE (formerly “Raptor Lake”) processor is based on Intel’s industry-leading silicon technology and the latest Performance Hybrid Architecture enhancements.

This 13th Generation processor marks the first Hybrid processor targeting embedded systems in Intel’s continual cadence for delivering the highest performance processors to the aerospace and defense industry. The processor delivers 50% more processing cores over 11th Gen Intel Core “Tiger Lake” processors, while still meeting the same low power levels required to support today’s size, weight, and power (SWaP) sensitive designs.

Safety Certifiability

The Intel Core i7-1376PRE is the latest processor from Intel powering avionics safety following on from the 11th Gen Intel Core Processor (formerly code-named “Tiger Lake UP3) with an Intel® Airworthiness Evidence Package (AEP) supporting DAL A.

The VPX3-1222/V3-1222 Circuit Board Assembly, COTS devices and custom devices meet the FAA-EASA

aligned means of compliance AC 20-152A/AMC 20-152A objectives. Process assurance covers DAL A with an artifact kit providing evidence required to be submitted to certification authorities.

SR-IOV Virtualization

SR-IOV (Single Root I/O virtualization) supported with Intel enablement toolkit, including the GPU.

Aligned with the SOSA® Technical Standard

After decades of dealing with proprietary point solutions, defense and aerospace organizations are facing significant interoperability, flexibility, and size, weight, power, and cost (SWaP-C) challenges. Technical standards like SOSA are designed specifically to alleviate these challenges and deliver a variety of benefits to C5ISR systems, including increased interoperability, elimination of vendor lock-in, simplified upgrades, and increased investment protection.

The VPX3-1222/V3-1222 is developed in alignment with the SOSA Technical Standard, with support for the 3U I/O Intensive SBC PIC profile. [Learn more about SOSA.](#)

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Hybrid Processor Architecture

The VPX3-1222/V3-1222 supports the Intel Hybrid Processor architecture, developed to meet the most demanding workload requirements by directing applications requiring high performance to higher Performance (P)-cores, while utilizing highly Efficient (E)-cores for less time-critical processing needs.

The i7-1376PRE processor offers 6 non-threaded P-cores plus 8 x E-cores for a total of 14-cores. P-cores offer the highest performance to handle complex workloads and E-cores excel at multi-threaded throughput, power-limited scenarios and applications looking for lockstep execution. All processing cores operate simultaneously.

[Learn about Intel Hybrid Processor Architectures](#)

Curtiss-Wright has a series of white papers detailing the performance and efficiencies of Hybrid processors, with example use-cases that greatly benefit the embedded Aerospace and Defense industry. Read the Cores & Threads white papers [Part 1](#) and [Part 2](#).

Dual Data Rate (DDR5) SDRAM

The VPX3-1222/V3-1222 has two independent 64-bit DDR5 SDRAM memory banks that are fitted with 64 GB total capacity. The DDR5 interface operates at 4,800 MT/s, yielding a memory throughput performance of 76.8 GB/s.

To preserve data integrity, the SDRAM is protected with in-band error-correction (ECC) circuitry.

NVMe SSD

The VPX3-1222/V3-1222 processor is configured with a high-performance non-volatile memory express (NVMe) to provide system flexibility for local storage connected directly to the processor, eliminating traditional performance bottlenecks associated with SATA connected storage. To provide system flexibility for local storage connected directly to the processor, eliminating traditional performance bottlenecks associated with SATA connected storage.

Fabric Ports

On the Expansion Plane, the VPX3-1222/V3-1222 provides 8-lanes of PCIe, used primarily to connect to adjacent VPX modules.

The PCIe port operates at Gen1 (2.5 GT/s), Gen2 (5 GT/s) and Gen3 (8 GT/s) speeds, for fast data transfers.

Common uses of the VPX Expansion Plane are to connect the processor to sensor or signal acquisition modules,

or to connect to dedicated FPGA modules offering additional computational power. The Expansion Plane can also connect to a central PCIe switch permitting PCIe expansion or high-speed data communications across the PCIe fabric.

Control and Data Plane Ethernet interfaces



The VPX3-1222/V3-1222 offers two SerDes Ethernet ports supporting 10GBASE-KR (10 GbE) and one 1000BASE-T port.

The 1000BASE-T port offers a range of Time Sensitive Networking (TSN) features, which adds real-time deterministic messaging capabilities to standard Ethernet networks. To make use of TSN features, a TSN capable Ethernet switch is required.

Additional I/O

In place of a XMC site, the module provides additional I/O to support a variety system applications.

Three additional 1000BASE-T Ethernet with TSN interface are provided which can be used with the primary 1000BASE-T Ethernet port to provide redundant TSN Ethernet capability.

A second DisplayPort graphics interface is provided limiting the need for complex FPGA processing to extract additional graphics channels from a Multi-Stream Transport (MST) protocol on the primary DisplayPort when more than one graphics output is required.

A dedicated 4-lane PCIe interface separate from the fabric PCIe interface, is provided. This interface may be used to connect to an external FPGA for low latency video capture and/or display controller and output formatting to provide further graphics outputs (may require graphics driver customization to support).

Four discrete digital I/O (DIO) signals in addition to the four base DIO signals.

An I2C interface for low complexity control of system backplane and/or I/O panel functions.

Serial Ports

The VPX3-1222/V3-1222 processor board provides one UART maintenance port operating at LVCMOS levels. A separate serial port operating as dual RS-232 is also supported.

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All serial ports support asynchronous communications with common baud rates configurable from 300 to 115,200 baud.

Discrete Digital I/O (DIO)/CardFail

The VPX3-1222/V3-1222 provides a total of eight independent discrete digital I/O signals. Each DIO is individually programmable as an input or an output. DIO's are capable of triggering an interrupt upon a change of state and are programmable to detect either rising or falling edge. All DIOs are 5V-tolerant.

One DIO output is dedicated to provide CardFail*, to indicate current overall status of Built-In-Test Equipment (BITE) and Built-In-Test Software (BIT).

BITE includes over temperature detection, watchdog timer, and other continuous hardware monitoring.

USB Ports

The VPX3-1222/V3-1222 provides one USB 2.0 and one USB 3.2 Gen 1 port.

SATA Ports

The VPX3-1222/V3-1222 provides one SATA 2.0 interface on the rear VPX backplane.

Table 1 DisplayPort Graphics Resolution

Display Config	Signal Rate (per lane)	Effective Data Rate (4-lane)	Max Resolution
DP 1.1 (HBR)	2.7 Gbps	8.64 Gbps	2560 x 1440 @ 75 Hz
DP 1.2 (HBR2)	5.4 Gbps	17.28 Gbps	3840 x 2160 @ 75 Hz

Display Interface

The processor supports an integrated Intel Iris Xe graphics engine, which operates with a base clock of 350 MHz.

The VPX3-1222/V3-1222 provides two 4-lane DisplayPort interfaces to the backplane and supports DisplayPort modes at up to HBR2 data rates with resolutions up to 4K60.

The Primary DisplayPort interface can also drive multiple monitors using the MST protocol.

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Integrated GPU

The integrated graphics engine can also provide GPGPU functionality, offering up to 536 GFLOPS of performance and usable by applications using a Vulkan programming interface.

Integrated Hardware Codec

The processor incorporates a hardware video codec, accelerating video compression and decompression algorithms and reducing CPU processing requirements. The codec supports MPEG, H.264 (AVC), H.265 (HEVC) and VP9 formats and features both 8-bit and 10-bit (HDR) image processing. Contact [CoreAVI](#) for latest driver supported accelerated codec features.

Failure Detection Coverage

A functional level Failure Modes and Effects Analysis (FMEA) is performed during design to derive additional hardware requirements for safety nets (BITE), identify module level BIT software, identify system level requirements, and provide a measure of failure mode detection coverage. The FMEA flows up to system engineering to support Functional Failure Path (FFP) analysis. The FMEA is tailorable at the system level to determine the specific functional attributes that are safety related and further to determine any specific anomalous behavior of those functions that would consist of a Level A and B FFP within the circuit/component.

Security Features

The VPX3-1222/V3-1222 is equipped with Trusted Computing features to protect against physical and remote attacks. For more information, see the [TrustedCOTS™ brochure](#). Due to the nature of trusted computing, not all security features are described here. Please [contact Curtiss-Wright](#) for additional security information.

Trusted Platform Module (TPM) support

The VPX3-1222/V3-1222 includes a Trusted Platform Module (TPM) 2.0 hardware security device which is compliant to FIPS-140-2 and is Common Criteria certified. The TPM can be used to create a secure computing environment, ensuring only trusted and signed software can execute on the board.

The TPM supports secure key storage, advanced cryptography algorithms, and other enhanced features.

Software Support

The VPX3/V3-1222 is supported with Rocky Linux and full source code can be purchased to support safety certifiable BSP development.

Built-in Test (BIT)

Built-in Test (BIT) is a library of diagnostic routines to support Power-On BIT (PBIT). BIT operations are supported through bootloader and software APIs and can be integrated into customer developed applications.

Operating System Software

Safety certifiable operating system support, bootloader, board support packages (BSP) and related DO-178C artifacts can be obtained directly from the selected RTOS vendor.

Graphics Driver

Safety certifiable OpenGL and Vulkan drivers for the integrated GPU can be obtained from CoreAVI with support for the chosen RTOS and with DO-178C Level A support.

VAPS software renderer from PACE Aerospace & IT offers HMI designers, systems engineers, and embedded engineers maximum control and flexibility for creating interactive real-time graphical displays for avionics and other safety-critical embedded applications. VAPS also simplifies the process for certifying a system up to DO-178 Dal A.

Software Maintenance

To keep pace with emerging requirements and security threats, Curtiss-Wright continues to maintain software updates over the full life-cycle of a product. Customers with an active support contract receive access to periodic updates that address potential vulnerabilities and maintain compliance with published specifications.

Rear Transition Module

For building development systems in a lab environment, Curtiss-Wright provides a Rear Transition Module which plugs into the backside of the VPX3-1222/V3-1222's backplane and provides access to many of the board I/O interfaces on industry standard connectors.

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Figure 2: RTM3-SBC rear transition module

VPX Slot Profiles

The VPX3-1222/V3-1222 is offered as a SOSA I/O Intensive Profile as shown in Figure 2. Meeting the VITA slot profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16, this profile populates the entire VPX connector with copper connectors to offer the widest number of interfaces, and supports XMC mezzanine I/O

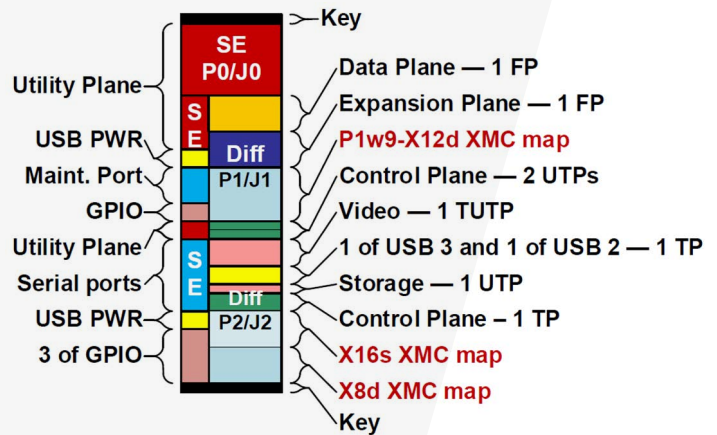


Figure 3: VITA/SOSA Profile SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16

Specifications

Form Factor

- 3U OpenVPX, developed in alignment with the SOSA Technical Standard
 - I/O Intensive SBC profile:
 - » SLT3-PAY-1F1F2U1TU1T1U1T-14.2.16
 - » MOD3-PAY-1F1F2U1TU1T1U1T-16.2.15-2

Processor

- 13th Gen Intel Core i7-1376PRE (formerly “Raptor Lake”) processor
 - 14-core processor, 28W TDP
 - » 6 x P-cores at 1.9 GHz
 - » 8 x E-cores at 1.2 GHz
 - Intel Advanced Vector Extensions (AVX, AVX2) floating-point
 - Intel Virtualization Technology (VT-x, VT-d) SR-IOV
 - Intel AI Acceleration with Deep Learning Boost (VNNI)
 - Intel Iris X^e Graphics with 96 EUs
 - Intel Multi-Key Total Memory Encryption (MK-TME)

SDRAM Memory

- 64 GB LPDDR5 at 4,800 MT/s
- Dual-channel memory configuration with IB-ECC and supporting MK-TME encryption

Non-volatile Memory

- 160 GB SSD
- 512 KB NVRAM
- 16 MB SPI flash for bootloader

Expansion Plane Fabric

- 8-lane PCIe Gen3 Expansion Plane

DP/CP Ethernet Ports

- 2 x 10GBASE-KR
- 2 x 1000BASE-T with support for the following TSN features:
 - 802.1AS-2020 Time synchronization for TSN
 - 802.1Qav Forwarding and queuing enhancements (credit-based shaping)
 - 802.1Qbv Time-aware shaping
 - 802.1Qbu, 802.3br Frame pre-emption
 - 802.1Qcc via Linux TSN software stack

Additional I/O

- 1 x UART maintenance port LVCMOS signal levels
- 2 x RS-232 serial UART channels
- 8 x Discrete I/O (one output dedicated to CardFail* function)
- 1 x USB 2.0 port
- 1 x USB 3.2 Gen 1
- 1x I²C
- 2 x DisplayPort interface supporting up to HBR2 rates
- 1x 4-lane PCIe interface for external video capture and/or display controller functions

Security Features

- Trusted Platform Module (TPM) 2.0 hardware device, compliant to FIPS and Common Criteria
- Intel MK-TME Multi-Key Total Memory Encryption

Software Support

- Rocky9.2 Linux supported
- Software updates can be downloaded from CSC when on maintenance
- Contact preferred RTOS vendor for BSP
- Contact CoreAVI for graphics drivers

Built-in Test

- Power-up BIT (PBIT)
- Hardware BITE functions including
 - Over temperature detection
 - Watchdog timer

Power

- Primary Power: Vs1 (+12V), 3.3V_AUX

Power Consumption

Power consumption will vary based on operational loading. Values below are guidelines for operation with 14 cores @ base frequencies at room temperature (25°C) – contact Curtiss-Wright for more details on power consumption.

- Idle power consumption = <TBD> watts
- Typical power consumption = <TBD> watts
- Maximum power consumption = <TBD> watts

Note: power consumption is exclusive of optional mezzanine power

VPX Connectors

- P0, P1, P2 = RT2 connectors

Environmental

- Conduction-cooled: Level 300 with 2LM covers
 - VPX3-1222 is designed to meet VITA 47.3 ECC4 (85°C)

Weight

- Conduction-cooled Level 300 TBD

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Ordering Information

V3-1222 boards described in this product sheet are orderable per below.

- All V3-1222 modules listed are conduction-cooled, L300 with 2LM covers
- Rear Transition Modules (RTM3-SBC) are air-cooled and support lab development

Table 2 VPX3-1222/V3-1222 Ordering Information, I/O Intensive Profile

Part Number	OpenVPX Profiles Supported
VPX3-1222-C252G50C00	13th Gen Intel Core i7-1376PRE Single Board Computer, I/O Intensive Profile with card edge temperature range -40 to +85C <ul style="list-style-type: none"> ▪ 64 GB DRAM
V3-1222-C952G50C00	13th Gen Intel Core i7-1376PRE Single Board Computer, I/O Intensive Profile with card edge temperature range -40 to +71C <ul style="list-style-type: none"> ▪ 64 GB DRAM
RTM3-SBC-0002	Rear Transition Module aligned with the SOSA Technical Standard, I/O Intensive Profile <ul style="list-style-type: none"> ▪ Provides breakout connectors and cables to most I/O interfaces ▪ Supports Curtiss-Wright RIM mezzanine module for XMC I/O breakout <ul style="list-style-type: none"> - RIM-GEN-0001 for low-speed signals - RIM-GEN-0002 for high-speed and differential signals
SCA-1222-2P00	Plan for Hardware Aspects of Certification (PHAC) for the V3-1222-C252G50C00. Includes system Integrator responsibilities to put into the context of a specific system (applies to all DAL levels)
SCA-1222-2A00	Certification artifacts required to be submitted to certification authority licensed for DAL A use of V3-1222-C252G50C00 (less the PHAC which is provided under SCA-1222-2P00)
SCA-1222-2C00	Certification artifacts required to be submitted to certification authority licensed for DAL C use of V3-1222-C252G50C00 (less the PHAC which is provided under SCA-1222-2P00)
SCA-1222-F000	Functional Failure Modes Effects Analysis (F-FMEA) for the V3-1222. Provided as a workbook to support tailoring based on system/application use of the V3-1222 in support of functional failure path analysis
DSW-1222-6920-RHL6	Rocky 9.2 BSP (64-bit)
MNT-1222-6920-RHL6	Annual support and maintenance for DSW-1222-6920-RHL6